



Technical delivery terms (TLB), recommendations and design rules for printed circuit boards

orgavision Export from 28.01.2026

Precoplat GmbH – Printed circuit boards made in Germany

Precoplat Präzisions-Leiterplatten-Technik GmbH is one of Germany's leading printed circuit board manufacturers. As a medium-sized family business, we have been manufacturing unassembled printed circuit boards at our production site in Krefeld, North Rhine-Westphalia, since the 1970s. 100% made in Germany.

At our approximately 25,000 m² company premises, more than 70 employees use highly technical and automated processes to produce over 100,000 m² of printed circuit boards per year. We supply a wide range of industries internationally and can respond quickly and flexibly to customer requests.

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1. Products

Our product range includes single-sided printed circuit boards, double-sided printed circuit boards and through-plated printed circuit boards, multilayers with up to 24 layers, and semi-flexible printed circuit boards from prototypes to (large) series production. Our processes are designed to ensure the highest quality and reliability. **PRECOPLAT is your expert printed circuit board manufacturer in Germany.**

For medium and large series of up to 25 m² per order, we offer an express service, which can be implemented as follows:

Type	Express	Average processing time
Standard* single- and double-sided PCBs	3 days	~ 12 days
Standard* Multilayer	4 days	~ 15 days

*Standard: 1-4-layer printed circuit board using hot air levelling technology, solder resist mask, FR4 material, conventional drilling techniques

Our service begins with technical support and extends to integration into our customers' supply chain management. We take every unique specification and individual requirement into account.

We always distinguish between three service categories: standard, special and technical limit.

2. Data

2. Data

Our CAM staff ensure that your layouts are implemented right through to the finished printed circuit board.

If you are unable to generate the files in the formats described, please contact our sales team.

You can send us your production data in the following formats:

2.1. Layout data

- Extended Gerber 274x (standard)
- Gerber 274
- Eagle
- Autodesk Fusion 360
- ODB

2.2. Drilling and milling data

- Excellon (standard)
- Drill file in Sieb & Meyer format 3000

Mechanical drawings can also be submitted in HPGL or DXF format.

3. Design rule check

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All data supplied to us is checked for manufacturability using a standard design rule check in accordance with IPC-2211 and customer-specific DFM functions. Additional services (e.g. impedance control, layout/data changes, reverse engineering) are provided on request and exclusively after separate commissioning.

3.1. HDI/Micro-Vias

For micro-vias (HDI), we follow **IPC-2221 / IPC-2226** and the **ZVEI design guidelines**. The following guidelines apply to the design rule check:

- Restriction on micro-vias: $\geq 100 \mu\text{m}$ (standard), $\geq 75 \mu\text{m}$ (special).
- Aspect ratio of micro-vias (drill depth \div hole diameter): $\leq 1 : 1$.
Example: Hole $\varnothing 100 \mu\text{m}$, drilling depth $63 \mu\text{m}$ \rightarrow AR = 0.63 : 1.

Note: Copper foil thickness according to [6.2. Standard copper foil thickness \(before electroplating\)](#), deviations are possible after prior consultation. For BGA / CSP / flip chip / COF, we take this into account in the design rule check and in the data check (including pad geometry, via-in-pad, restring, solder resist, distances).

3.2. Optional engineering lines

Software-supported impedance control (= in-depth control): Creation of a polar report (calculation/validation) based on the approved layer structure; target values and tolerances according to customer specifications.

Reverse engineering (reading of submitted printed circuit boards): Recording of the layer structure, capture of conductor pattern/drilling data/network information and reconstruction of CAM-compatible manufacturing data (e.g. Gerber/ODB++); implementation only with usage rights clarified by the client.

4. Quality

4.1. Quality standards

We manufacture **unassembled printed circuit boards in accordance with IPC-6012 (including addendum – Space and Military/Medical (on request)), Class 2 or Class 3. Acceptance is carried out in accordance with IPC-A-600, Class 2 or Class 3.**

In addition, we support the following standards/specifications on request:

- Solder resist (material/qualification): **IPC-SM-840**
- Final surface (ENIG): **IPC-4552**
- Design basics (customer layout): **IPC-2221**
- HDI/Micro-Vias Design (customer layout): **IPC-2226**
- **PERFAG** (European specification for delivery agreements & quality levels)
 - PERFAG 1 – single-sided
 - PERFAG 2 – double-sided
 - PERFAG 3 – multilayer

Semiflex (FR4 thinned, "flex-to-install"): Manufactured as a rigid printed circuit board in accordance with IPC-6012; acceptance in accordance with IPC-A-600; not an IPC-6013 product.

Revision valid on the date of order confirmation.

4.2. Quality assurance

We comply with UL® standards and RoHS directives and are certified according to DIN EN ISO 9001. Production parameters, production conditions and raw materials are evaluated and recorded using calibrated measuring instruments.

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The printed circuit boards are subjected to the following tests during the production process to ensure flawless quality:

Non-destructive testing

For optical inspections, we use IPC-A-600 as an image reference; acceptance is based on the class ordered (class 2/3). AOI minimum structure: 25 µ. Specific test procedures can also be adapted to other specifications at any time if required.

Destructive testing

- Micrograph preparation,
- adhesion test,
- delamination test (multilayers are regularly subjected to thermal shock tests).

Documentation of parameters

Automatic recording and storage of the following parameters for at least 10 years:

- Production parameters,
- Quality-related results,
- Time recording, including the respective employees.

X-ray

X-ray fluorescence spectrometry for layer registration and layer thickness measurement.

AQAP

AQAP-2110 requirements are implemented internally. For projects subject to AQAP, we plan the official quality assessment (GQA) and apply for BAAINBw confirmation on a project-specific basis.

5. Electrical testing

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During the final electrical test, printed circuit boards are checked for interruptions and short circuits.

The client's Gerber data is loaded into our test system, which generates a net list containing all identified test points. These test systems test according to the following criteria as standard:

- for interruptions, if > 10 ohms network resistance is detected
- for short circuits if resistances < 10 megohms are detected between independent shunts

We use the following test systems:

5.1. Test adapter/parallel tester

Based on the test programme, adapter plates are drilled and equipped with test needles, which are deflected to the relevant contact points in order to simultaneously detect all end points of the electronic network for the test process for short circuits and interruptions. At the same time, all networks are tested against each other. The test result is then compared with the electrical network list.

5.2. Finger tester (flying probe)

Alternatively, the electrical test can be performed using a finger tester. The contact points on the circuit board are sequentially contacted with contact needles based on the underlying network list and tested for continuity and interruption. The measuring needles are attached to mechanically movable "fingers" which move to the previously programmed test positions.

In all test procedures, the printed circuit boards on which a short circuit or interruption has been detected are automatically separated from the clearly fault-free printed circuit boards. For faulty or unclearly tested printed circuit boards, an error log with the exact error position is created. After successful troubleshooting, the printed circuit board is subjected to a complete test run again.

6. Base material

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The CAF (Conductive Anodic Filament) resistant FR4 base material is permanently in stock.

- in thicknesses from 0.5 to 3.2 mm
- Creepage current resistance (CTI) values up to 600 volts
- TG value up to 170 degrees Celsius

Directly available:

- **FR4 TG 135°-140°; CTI 175-249 (standard)**
- FR4 TG 150°
- FR4 TG 170°
- FR4 CTI 250-399 PLC 2
- FR4 CTI 400-599 PLC 1
- FR4 CTI ≥ 600 PLC 0
- CEM1
- CEM3

In addition, we can procure other base materials of various thicknesses on request.

6.1. Material properties

The following values apply to material thicknesses from 0.5 mm:

Laminate	NEMA	IPC-4101	Tg C°	CTE < Tg ppm/K	CTE > Tg ppm/K	Decomposition temperature C°	T260 min	T288 min	
epoxy-paper-glass	CEM1	10	100	-	-	-	-	-	
epoxy-glass	FR4.0	21	135	70	280	310	20	2	Standard
epoxy-glass	FR4.0	99	150	60	250	350	60	20	High Tg inorganic fillers
epoxy glass	FR4.0	101	170	60	230	350	60	20	Higher Tg inorganic fillers
epoxy glass	FR4.1	128	150	50	230	340	60	20	Halogen-free inorganic fillers
epoxy glass	FR4.1	130	170	50	230	350	60	20	Higher Tg Halogen-free inorganic fillers

6.2. Copper foil thickness Standard (before electroplating)

18 μ	35 μ	50 μ	70 μ	85 μ	105 μ
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6.3. Copper-clad laminates

FR4 in mm		FR4 CTI > 400	CEM 1 (on request)	CEM 3 (on request)
0.10	plus Cu	1.0	1.00	1.55
0.20	plus Cu			
0.25	plus Cu			
0.36	plus Cu			
0.41	plus Cu			
0.50	plus Cu			
0.71	plus Cu	1.55	1.55	
1.00	incl. Cu			
1.08	plus Cu			
1.55	incl. Cu			
2.00	incl. Cu			
2.40	incl. Cu			
3.00	incl. Cu			

7. Tolerances for warping and buckling

One side	Double-sided	Multilayer
1.5	1	1

Please note that the warpage value increases above average if the copper distribution on the printed circuit board varies greatly in certain areas. Especially with multilayers, a symmetrical layer structure should be planned right at the start of layout development. With asymmetrical material structures, the different tensions of the glass fabric qualities can result in higher torsion and warpage values.

8. Available production benefits

In order to manufacture economically and sustainably, we examine the best possible utilisation of our production capacity and compare this with the most frequently used PCB sizes to avoid unnecessary waste.

	Single-sided printed circuit boards mm		Double-sided printed circuit boards mm		4-layer PCB standard structure MassLam mm		4-layer PCB with over 6 prepregs and 6-24 layers PCB PinLam mm	
	Length	Width	Length	Width	Length	Width	Length	Width
Panel size 1	618	512	614	512	614	512	600	499
Panel size 2	Not available		584	512	584	512	Not available	
Panel size 3	584	436	Not available		Not available		Not available	

9. PCB thickness

We can process different PCB thicknesses regardless of the number of layers.

Lead times for special material thicknesses may vary if the desired material is not in stock.

	Standard mm	Special mm	Technical limit Single and double-sided mm	Technical limit Multilayer mm
Min. panel thickness	1.55	0.8	0.4	0.4
Max. panel thickness	1.55	2.4	3.2	3.2

10. Multilayer layers and structures

10. Multilayer layers and structures

Multilayers consist of copper layers, prepregs and thin laminates. These can be combined in completely different ways, resulting in an infinite variety of construction options. We manufacture multilayers with up to 24 layers. The layers can then be connected via through-plating between the outer layers (vias), from an outer layer to an inner layer (blind vias or blind holes) or between the inner layers (buried vias).

The most commonly used layer structures can be found on our website in the Download Centre.

Of course, if you have any questions, you are also welcome to contact our sales team directly. We will be happy to send you special layer structures on request.

The following basic principles should be observed when creating a multilayer layout:

10.1. Symmetry

A symmetrical material structure should be planned right from the initial design stage, taking into account identical thin laminates and prepreg types in the same order. Among other things, this significantly reduces warping and buckling (stresses released by thermal and mechanical effects during the manufacturing process and use).

10.2. Consideration of physical influencing factors

For some special designs, the material structure (stack-up) of a multilayer is particularly crucial. The choice of layer structure depends on various physical influencing factors.

The most important parameters are:

- Dielectric strength of the layers in relation to each other
- Permittivity ϵ (dielectric conductivity) / "Dk" of the base material (also dielectric constant) with loss factor "Df"
- Temperature and moisture content

Dielectric strength

For FR4 base material of 0.5 mm, laminate manufacturers specify a dielectric strength of 800 V - 1200 V/25 μ . However, in practice, the actual remaining insulation layer between the layers is smaller, as prepregs embed themselves into the copper structures during pressing. Thin laminates are recommended, as their thickness change after pressing is negligible.

Please note that the test procedures for determining dielectric strength according to the IPC standard refer to unlaminated materials. The dielectric strength of a complete multilayer is not taken into account. We therefore recommend a sufficient safety margin.

When starting the layout design of your multilayer, we advise you to follow the provisions of the IEC, VDE and UL® standards, which contain specifications for sufficient insulation between adjacent conductors.

Permittivity ϵ

The thickness and quality of the dielectric (prepreg) between the copper layers influence the capacity and impedance of the printed circuit board.

Physical values of common FR4 prepregs:

Prepreg type	Thickness in μ (before pressing)	Thickness in μ (after pressing)	Resin content	Tolerance in %	1 MHz		1 GHz		5 GHz		10 GHz	
					Dk	Df	Dk	Df	Dk	Df	Dk	Df
1080	approx. 75	approx. 70	\emptyset 62	+/- 3	3.90	0.017	3.76	0.019	3.72	0.020	3.69	0.020
2116	approx. 120	approx. 115	\emptyset 50	+/- 3	4.30	0.016	4.18	0.018	4.15	0.019	4.12	0.019
7628	approx. 190	approx. 180	\emptyset 43	+/- 3	4.60	0.017	4.36	0.018	4.34	0.019	4.31	0.019

Physical properties of common FR4 thin laminates:

Number of prepregs	Thickness in μ	Resin content	Tolerance in μ	1 MHz		1 GHz		5 GHz		10 GHz	
				Dk	Df	Dk	Df	Dk	Df	Dk	Df
1 x 2116	110	\emptyset 44.5%	+/- 18	3.93	0.020	4.11	0.017	4.03	0.018	3.97	0.018
1 x 7628	200	\emptyset 44.0	+/- 25	4.13	0.019	4.12	0.017	3.96	0.018	3.98	0.018
2 x 7628	360	\emptyset 39.5%	+/- 38	4.70	0.017	4.21	0.017	4.05	0.018	4.09	0.018
2 x 7628	410	\emptyset 42.5%	+/- 38	4.40	0.019	4.12	0.017	3.96	0.018	3.98	0.018
3 x 7628	500	\emptyset 39.5%	+/- 50	4.70	0.017	4.25	0.017	4.10	0.018	4.14	0.018
4 x 7628	710	\emptyset 39.0	+/- 50	4.70	0.017	4.25	0.018	4.10	0.019	4.14	0.019

Temperature and moisture content

Please allow for the following tolerances:

- The Dk value increases by approx. 17% after moisture absorption for typical standard FR4.
- The Df value increases by approx. 12% after moisture absorption for typical standard FR4.

Please note that thermal stress, such as that caused by soldering processes and thermal cycles, which the circuit board experiences during manufacture and use, can also have an impact on the electrical and mechanical properties of the material. Increased temperature leads to thermal expansion, which can result in mechanical stresses and potential defects such as delamination or microcracks. These effects can compromise the reliability and longevity of the PCB. Therefore, when planning the multilayer structure, the thermal stresses to which the PCB will be exposed during use should also be taken into account.

A well-thought-out layer structure and the choice of suitable materials can help to minimise thermal stresses and extend the service life of the printed circuit board:

- **High-temperature-resistant materials:** High-quality prepregs and laminates from the best manufacturers are more resistant to thermal stresses.

- **Reinforced prepregs:** Prepregs with a high glass content offer better mechanical properties and higher thermal stability.
- **Symmetrical structure:** A symmetrical layer structure helps to distribute mechanical stresses evenly and minimise warping.
- **Optimised layer thicknesses:** Plan the thicknesses of the prepregs and laminates so that thermal expansion is minimised.
- **Sufficient spacing:** Ensure that there is sufficient space between the copper layers to accommodate thermal expansion and prevent delamination.

By carefully considering these factors, you can significantly improve the performance and longevity of your multilayer printed circuit boards.

If you have any further questions, please contact our sales department or our work preparation team. They can also provide you with layer structure samples.

11. Circuit pattern creation

The lithographic limit for the resolution of conductor patterns (track/gap) in the exposure systems we use is the thickness of the dry resist to be exposed. If this has a thickness of 50 µ, the maximum possible resolution is also 50 µ. Physical processes in the subsequent electroplating and etching processes also have a limiting effect. The higher the final copper thickness, the higher the degree of under-etching at the edges, which must be compensated for in the exposure parameters.

Basically, the reproducibility of a layout depends on its design and the thickness of the copper build-up. The technical restrictions of solder resist production must also be taken into account. When creating and editing layouts, it is necessary to consider questions regarding the coverage, undercoverage or even exposure of the conductor flanks and insulation areas.

Final copper thickness 35 µ	Standard µ		Special µ		Technical limit µ	
	Outer layers	Inner layers	External layers	Inner layers	External layers	Inner layers
Conductor track width	120	120	100	100	60	60
Conductor track spacing	120	120	100	100	70	70
Restrings	125	150	100	120	70	80
Registration accuracy	+/- 20 µ		+/- 15 µ		+/- 12 µ	
Final copper thickness 70 µ	Standard µ		Special µ		Technical limit µ	
	Outer layers	Inner layers	External layers	Inner layers	External layers	Inner layers
Conductor track width	150	150	125	125	100	100
Conductor track spacing	170	170	140	140	120	120
Restrings	180	200	150	170	120	120
Registration accuracy	+/- 20 µ		+/- 15 µ		+/- 12 µ	

End copper thickness 105 µ	Standard µ		Special µ		Technical limit µ	
	Outer layers	Inner layers	External layers	Inner layers	External layers	Inner layers
Conductor track width	200	200	170	170	130	130
Conductor track spacing	250	250	225	225	200	200
Restring	250	275	200	225	150	175
Registration accuracy	+/- 20 µ		+/- 15 µ		+/- 12 µ	

End copper thickness 140 µ	Standard µ		Special µ		Technical limit µ	
	Outer layers	Inner layers	External layers	Inner layers	External layers	Inner layers
Conductor track width	300	300	250	250	230	230
Conductor track spacing	400	400	360	360	320	320
Restring	300	300	270	270	250	250
Registration accuracy	+/- 20 µ		+/- 15 µ		+/- 12 µ	

12. Solder resist mask

12th solder resist mask

In the phototechnical solder resist process, the surface is embedded in a photosensitive polymer. The chemical cross-linking of the polymers is achieved by defined exposure; all unexposed areas are developed with sharp contours, even in the micrometer range. In order to achieve the required electro-physical properties of the coating, a UV bump is then applied, which essentially "glazes" the coating surface to reduce ionic contamination, followed by final thermal curing.

During solder resist coating, the solder eyes of the via holes can be printed over on request. However, this does not guarantee that the via holes will be sealed (via plugging) (not suitable for vacuum testers).

If it is absolutely necessary to seal the via holes, this process is carried out in a separate procedure in which the holes in question are specially coated with lacquer and sealed.

Standard lacquers can be used to seal holes with a diameter of up to 0.45 mm. For larger hole diameters, a special lacquer or resin filling is required.

12.1. Parameters for exemption and expansion of solder resist

We only use epoxy resin-based solder resist, as this also improves the creepage resistance on the surface of the printed circuit boards.

Values apply to green solder resist	Standard µ	Special µ	Technical limit µ
Approx. expansion of the solder resist mask	70	50	30
Minimum web width	80	60	50
Min. distance between SMDs*	200	170	150
Registration accuracy green/other	+/- 20/40 µ	+/- 15/35 µ	+/- 12/30 µ

*Minimum distance between solder resist-free areas in order to reproduce a solder resist bridge

When creating solder resist masks, solder resist exemptions must be taken into account in a 1:1 ratio to the pads, i.e. without oversizing. We calculate the oversizing required for production ourselves.

The following solder resist colours are available:

- **green (standard)**
- blue
- black
- red
- white

TOP/BOTTOM can be painted differently.

13. Electroplating copper deposition process

13. Electroplating copper deposition process

The thickness of the copper plating depends on the exposure time and the current strength in the electroplating bath.

During the process, a layer of 20 µ to 25 µ copper is generally deposited on the surface and in the through-holes. Thicker copper layers are possible by adjusting the process parameters or using additional electroplating processes.

In order to achieve uniform copper deposition, the layout design should take into account that conductor track structures should either not be embedded in ground at all or be completely embedded in ground. The conductor tracks or pad positions should be centred within a ground embedding and spaced at equal distances from each other. If copper structures are unevenly distributed in the layout, there is a tendency for over-deposition in the "low ground" regions. This leads to a reduction in conductor track spacing and, ultimately, to electrical failure due to short circuits, as the conductor tracks literally grow together. For micro-vias (unfilled): metallisation in the hole $\geq 12 \mu$ (guideline value).

Copper foil µ	Electrolytic copper deposition	Final copper thickness
18 µ	approx. 20 µ	approx. 35 µ
35 µ		approx. 55 µ
50 µ		approx. 70 µ
70 µ		approx. 90 µ
85 µ		approx. 105 µ
105 µ		approx. 125 µ

13.1. Aspect ratio

For through holes and buried vias, the ratio of "material thickness to hole diameter" is defined. It is calculated as follows: material thickness divided by the smallest hole diameter.

Example: 1.6 mm material thickness divided by 0.2 mm hole diameter = 8

Standard	Special	Technical limit
8	10	> 10

This value is very important for the manufacturability of the printed circuit board, because the larger the aspect ratio, the more difficult it is to produce metallisation in the holes.

For blind vias and micro vias, the aspect ratio is calculated as the drilling depth (layer spacing) ÷ hole diameter; limit value $\leq 1 : 1$.

13.2. Microfilling (via-in-pad)

This technology enables the simultaneous filling of blind vias and the reinforcement of through holes.

In HDI circuits, there is usually not enough space to route the signals to different layers via through holes. A space-saving solution is via-in-pad: blind vias are positioned directly in SMD pads and filled with copper after drilling; the planarised surface supports the soldering process. Example (fine pitch): BGA/CSP/flip chip zones with via-in-pad for short transitions and even paste distribution. Due to this filling, only a very small amount of solder flows into the remaining "dimple" and enables a proper solder joint. Target value for the dimple: $\leq 25 \mu$. (Guideline value according to ZVEI). The maximum drilling diameter is 0.15 mm.

13.3. Via plugging using resin filling (also suitable for via-in-pad technology)

Sealing both through and blind vias with resin followed by subsequent over-metallisation is an alternative to microfilling, but this process is more complex in terms of process technology.

The advantages over microfilling are that

- through holes from 0.1 mm to 2 mm can also be closed; however, the material thickness must not be smaller than the drill diameter.
- Planar sealing of the holes is possible; no dimples remain in the pad.

14. Surface finishing

We can currently offer you the following surface finishes:

- Lead-free hot air tin plating (HAL) – Sn / 0.3 Ag / 0.7 Cu / 0.02 Ni
- Electroless nickel-gold (ENIG) – 99.9 Au
- Electroless nickel-palladium-gold (ENEPIG)
- Electroless tin (chem. Sn)
- Electroless silver (chem. Ag)
- Organic surface protection (OSP)
- Electroplated nickel-gold (hard and bond gold) – hard 99.8 Au / soft 99.99 Au

Properties of the various final surfaces:

	HAL	ENIG	ENEPIG	Chemical Sn	chem. Ag	OSP	galvanic Au
Layer thickness μ	< 10	0.05-0.12 Au 4-8 Ni	0.03-0.10 Au 3-7 Ni 0.08-0.30 Pd	0.80-1.20	0.15-0.45	0.02-0.06	0.80-5.00
Flatness	+	+++	+++	+++	+++	+++	+++
Shelf life under stable conditions	< 12 months	< 12 months	< 12 months	< 6 months	< 6 months	< 6 months	< 12 months
Multiple solderability	+++	+++	+++	+	++	o	yes (soft)
Reactivable	yes	Conditional	Conditional	yes	yes	yes	no
Al-wire bonding	no	yes	yes	no	Conditional	no	yes (soft)
Au wire bonding	no	no	no	no	no	no	yes (soft)
Push button contact	no	yes	yes	no	no	no	yes
Press-fit technology	yes	no	no	yes	yes	no	Nno

15. Printing techniques

15.1. Serialisation

To ensure that printed circuit boards can be clearly identified, individualised marking of the individual printed circuit boards within a series is also an option. This marking is applied automatically (direct exposure of the structures or assembly printing) in white and can consist of static information (e.g. production date, date code, etc.) and consecutive numbering in chronological order and can be displayed in the following machine-readable formats:

- 1D & 2D barcodes, data matrix, QR codes.

15.2. Marking printing / assembly printing

To avoid interruptions or obscuring within the typeface, the line thickness of the marking print should not be less than 130 μ and the font height should not be less than 1000 μ . The soldering areas should be left free of the marking print by at least 250 μ all around, as otherwise an unclean print image and pressure on the soldering areas is possible.

	Standard μ	Special μ	Technical limit μ
Distance between print image and pad	200	150	100
Distance between print image and holes	200	150	100
Line thickness	130	100	75
Font size	1000	750	500
Registration accuracy	+/- 200 μ	+/- 150 μ	+/- 70 μ

15.3. Carbon printing

	Standard μ	Special μ	Technical limit μ
Distance between carbon surfaces	500	400	300
Minimum width of carbon surface	700	600	500
Registration accuracy	+/- 250 μ	+/- 200 μ	+/- 150 μ

15.4. Removable coating

The layer thickness of the release coating is approx. 500 μ .

Holes covered with peel-off lacquer should not exceed a size of 1.8 mm.

	Standard	Special	Technical limit
Maximum diameter that can be covered	1.8 mm	2.0 mm	2.6 mm*
Minimum width	6 mm	5 mm	4 mm
Registration accuracy	+/- 300 μ	+/- 250 μ	+/- 200 μ

*Complete spanning of the hole cannot be guaranteed.

16. Contour machining

16. Contour machining

We drill, mill and score your printed circuit boards according to your specifications and requirements. The type of mechanical processing depends on your individual specifications. In our drilling and milling centre, we work with modern, fully automatic CNC drilling and milling machines. These techniques enable machining within the DIN 7168 standard "medium" (medium accuracy) and "fine" (precise accuracy).

If non-plated holes are positioned in a solder pad, the solder pad must be at least 500 µ larger than the hole. Otherwise, solder pads may be removed.

If no information about the type of holes is available for through-plated printed circuit boards, we will determine independently and to the best of our knowledge which holes are to be through-plated and which are not.

If drilling or dimensional plans are provided that do not correspond to the drilling programmes or the contour according to the layout data, the drilling programmes and the contour according to the layout data are binding for production in all cases.

Unless otherwise specified, the centre point (= centre vector) of the contour lines in the layout data is decisive for the contour of the printed circuit board. If slot milling (slots) is represented by rectangular contours, we assume that the corner radius is included.

Depending on the size of the printed circuit boards, the following tolerances are specified (other tolerance values are possible by agreement):

Format mm	Centre mm	Fine mm
0.5	+/- 0.10	+/- 0.05
6	+/- 0.20	+/- 0.10
30-120	+/- 0.30	+/- 0.15
120-400	+/- 0.50	+/- 0.20
400-1,000	+/- 0.80	+/- 0.30

16.1. Scribing (groove milling)

The angle of the scoring knives is 15°. Therefore, along the contours that are scored, a distance between the conductor tracks and the contour must be taken into account in accordance with the following table:

Material thickness mm	Distance between conductor tracks and contour mm
up to 1.00	0.45
1.10 - 1.60	0.5
1.70 - 2.00	0.70
2.10 - 2.50	0.8
2.60 - 3.20	1.0

If no positive tolerance is permitted for the contour, the desired negative tolerance must be added to the above values for "Distance between conductor tracks and contour".

Example: PCB format 100 mm x 100 mm +0.00/-0.30 mm

Distance between conductor tracks and contour with 1.6 mm material thickness: 0.5 mm + 0.15 mm = 0.65 mm

16.2. Milling

As an alternative to scribing, we offer contour milling. The advantage over scribing is that the outer contours can be machined in the most specialised shapes and cut-outs, such as round, oval, wave form, zigzag, etc.

When milling, please note:

- If delivery is to be made in milled panels, a standard spacing of 2.0 mm between the circuit boards is sufficient to allow milling bridges to be placed between the individual boards.
- If delivery is not to be made in sheets, a distance of at least 8.0 mm from board to board must be taken into account in order to ultimately be able to separate the circuit boards.

16.3. Deep milling and drilling / countersinking

Milling and drilling with a defined Z-axis is carried out according to your drawing specifications. Countersinks are produced at 45° or 30° as standard. The specifications for this can be determined individually.

16.4. Milling and scribing combination

In some cases, it makes sense to combine both milling and scribing in order to achieve the best compromise between cost and material loss. Our CNC machines are capable of implementing these combinations with precision.

16.5. Chamfering

For easier assembly of plug contacts (e.g. PCI connectors), edge chamfering at 45° or 30° is possible at various depths.

16.6. Edge metallisation

To create flank contacts, we can produce special edge metallisation (e.g. side plating or castellated holes). This is particularly useful when improved electrical conductivity or shielding is required.

16.7. Semiflex

With Semiflex technology, a defined area of rigid printed circuit boards is milled down to a residual material thickness so that the material can be bent there. Although the bending angles and radii achievable are not the same as with rigid-flex circuits, they are often sufficient for the applications. Depending on the design, the Semiflex technique allows three to five bends; the printed circuit board must therefore be mounted statically.

The main advantages are lower manufacturing costs and the elimination of the otherwise necessary polyimide film, which in turn would require thermal pre-treatment due to its high moisture absorption.

17. Drilling and milling tolerances

Plated-through holes (PTH)		Standard mm	Special mm	Technical limit mm
Smallest drill diameter		0.35	0.15	0.10
Largest drilling diameter		6.0	6.0	6.0
Smallest distance between drill tangents*		0.20	0.15	0.075
Smallest distance between drill tangents and conductor track*	Outer layers	0.2	0.15	0.075
	Inner layers	0.25	0.20	0.10

Surface Hot air levelling Tin plating	Final diameter <= 6 mm	+0.10/-0.05	+0.09/-0.06	+0.08/-0.05
	Tolerance	Final diameter > 6 mm milled	+0.14/-0.05	+0.10/-0.05
Surface OSP/ENIG/chemical tin/silver	Final diameter <= 6 mm	+0.10	+0.05/-0.05	+0.10
	Tolerance	Final diameter > 6 mm milled	+0.12/-0.02	+0.06/-0.06

Hole position tolerance of plated-through holes to non-plated-through holes and to the contour	+/-0.20	+/-0.07 **	+/-0.05
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Non-plated through holes (NPTH)		Standard mm	Special mm	Technical limit mm
Smallest hole diameter		0.40	0.20	0.15
Largest drilling diameter		6.40	6.40	6.40
Smallest distance between drill tangents*		0.20	0.15	0.1
Smallest distance between drill tangents and conductor track*	Outer layers	0.2	0.15	0.05
	Inner layers	0.25	0.20	0.10
Tolerance	Final diameter <= 2 mm	+/-0.05	+/-0.03	+/-0.03
	Final diameter 2 <= 6 mm	+0.1/-0.05	+/-0.05	+/-0.03
	End diameter > 6 mm milled	+0.1/-0.05	+/-0.06	+/-0.04

*Please note that plated-through holes usually need to be drilled or milled 150 µ larger than the desired final diameter in order to compensate for the metallisation in the hole. For example, if you want a final diameter of 0.6 mm, the diameter of the drill bit used is 0.75 mm, unless different tolerances are specified.

**depending on the hole diameter

***provided that the drilling process is carried out in a machine clamping (tenting)

18. Storage

18.1. Humidity

Due to the epoxy resin in the base material of the printed circuit boards, these (especially multilayer boards) are extremely hydrophilic; i.e. the water molecules dissolved in the air are absorbed by the material. Depending on the ambient conditions, moisture equilibria are established in the materials. Under storage conditions of, for example, 20 degrees Celsius and 35 per cent humidity, moisture absorption of 0.12 per cent (as a percentage by weight of the epoxy resin) is already recorded after 12 days. The decisive factor here is that as moisture absorption increases, so does the gas pressure inside the printed circuit board, which is caused by the high temperatures during the soldering process. If moisture absorption exceeds 0.17 per cent, a critical gas pressure of 8–10 bar is reached, which can lead to delamination and blistering. Epoxy resin can absorb up to 0.5 per cent moisture by weight.

To ensure that the moisture content and adhesive bond of the material are flawless, we perform a delamination test on a test specimen after completing multilayer printed circuit boards.

To further prevent or reduce moisture absorption, we strongly recommend the following points:

Storage environment

PCBs should be stored in a constantly heated environment under controlled conditions, preferably in darkened rooms, until shortly before soldering/processing. Due to climatic changes, a controlled storage environment is becoming increasingly important in order to maintain the quality of the printed circuit boards. Humidity and temperature fluctuations should be minimised and the packaging of the printed circuit boards must be checked for integrity before processing.

We strongly recommend that you adhere to the following conditions in the storage environment in order to minimise moisture absorption:

- Room temperature 18-21 °C
- Relative humidity < 50%

Packaging

Preferably, storage should be in closed containers. Please note that polyethylene bags do not provide reliable protection against moisture due to their water vapour permeability. To improve protection, we therefore also offer to pack the printed circuit boards in DRY-SHIELD protective bags. It is also possible to vacuum seal them and/or provide them with indicators and desiccant bags. The protective films/bags should only be removed shortly before soldering/processing. We recommend vacuum sealing any remaining quantities, or at least sealing them securely with adhesive tape or by clamping the film between the circuit boards, and storing them in boxes to prevent draughts.

Storage time

The storage time for printed circuit boards should be as short as possible and consumption should follow the "first in, first out" rule. For storage times of more than 3 months (based on the production period), it is difficult to predict when moisture absorption may lead to problems during soldering/processing due to a wide variety of influencing parameters such as layout, layer structure, etc. For reliable verification of the storage period, we can apply a production date/date code to the printed circuit boards by arrangement. Please note that the shelf life also depends on the selected final surface finish. You will find guidance values for this in the Surface Finishing section of this document. Please always use opened packages first.

18.2. Soldering test

Printed circuit boards that have been stored for several months and whose transport conditions are unclear (transport of goods by freight forwarders in all weather and temperature conditions) should always be subjected to a soldering test before further processing.

18.3. Preconditioning/drying

In order to reduce the amount of moisture absorbed, we recommend drying the goods in an oven, regardless of the outcome of a solder test, whereby the printed circuit boards should preferably be dried vertically in a rack. If you store the printed circuit boards with us for more than four months (e.g. for call-off orders), we will dry them before delivery in any case.

Degree °C	Drying time
120	4 hours
110	6 hours
100	8 hours

If drying in a vacuum oven at 50 mbar is possible, the temperature can be reduced by approx. 20 °C and the time by approx. 30 minutes. This process is advantageous for the sensitive "chemical tin" surface. Subsequently, a few test specimens should be used to determine whether the solder still wets sufficiently; otherwise, the chemical tin must be refreshed.

After drying, processing of the printed circuit boards should begin immediately, as the hydrophilic properties of the printed circuit board remain. The time between the various soldering processes must be kept as short as possible and should not exceed 8 hours. This is the only way to avoid excessive moisture absorption in unprotected material. Dried and tempered printed circuit boards will quickly become saturated with water from the ambient air.

18.4. Product-specific requirements

The values mentioned in the previous sections are guidelines.

The values do not take into account the different processing parameters and product-specific properties of individual printed circuit boards and must be determined by the respective processor on a product-specific basis:

- The various soldering processes and profiles cause different stresses. For example, the thermal stress in convection ovens is not as high as in infrared ovens or vapour phases.
- If the recommended storage conditions cannot be maintained consistently, the material will absorb more water than is possible under constant conditions. Packaging in DRY-SHIELD protective bags can help here.
- If the layout contains large, closed copper areas, it takes longer for the moisture to escape.
- The multilayer structure. See: [10.2. Consideration of physical influencing factors](#)