Technical delivery terms (TLB), recommendations and design rules for printed circuit boards

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Precoplat GmbH - Printed circuit boards made in Germany

Precoplat Präzisions-Leiterplatten-Technik GmbH is one of the leading PCB manufacturers in Germany. As a medium-sized family business, we have been manufacturing bare printed circuit boards at our production site in Krefeld, North Rhine-Westphalia, since the 1970s. 100 % Made in Germany.

On our 25,000 m² site, over 70 employees produce more than 100,000 m² of printed circuit boards per year in a highly technical and automated process. We supply a wide range of industries internationally and can react quickly and flexibly to customer requirements.

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1. Products

Our product range includes single-sided PCBs, double-sided PCBs and through-hole PCBs, multilayers with up to 24 layers as well as semi-flexible PCBs from prototype to (mass) production. Our processes are designed to guarantee the highest quality and reliability. **PRECOPLAT is your competent PCB manufacturer in Germany.**

For medium and large series of up to 25 m² per order, we offer an express service that can be realised as follows:

Type	Rush	Ø Processing time
Standard* single and double-sided LP	3 days	~ 12 days
Standard* Multilayer	4 days	~ 15 days

*Standard: 1-4-layer PCB in hot air levelling technology, solder mask, FR4 material, conventional drilling techniques

Our service begins with technical support and continues through to integration into our customers' supply chain management. We take every unique specification and individual requirement into account.

In the following, we always differentiate between three performance categories: Standard, special and technical limit.

2. Data

Our CAM employees ensure that your layouts are realised through to the finished PCB.

If you are unable to generate the files in the formats described, please contact our sales team.

You can send us your production data in the following formats:

2.1 Layout data

- Extended Gerber 274x (Standard)
- Gerber 274
- Eagle
- Autodesk Fusion 360
- ODB++

2.2 Drilling and milling data

- Excellon (Standard)
- Drill file in Sieb & Meyer format 3000

Mechanical drawings can also be transmitted in HPGL or DXF format.

3. Design rule check

All data supplied to us is checked for manufacturability using a standard design rule check and customised DFM functions. If this is not the case, we will contact you immediately.

4. Quality

4.1 Quality standards

We manufacture printed circuit boards in accordance with the **IPC-A-600 Class 2 or Class 3 standard.**

We can also produce to the following standards:

- PERFAG 1
- PERFAG 2
- PERFAG 3
- IPC-SM-840
- IPC-R-700
- IPC-A-600
- IPC-6012
- IPC-2221

4.2 Quality assurance

We fulfil the UL® standards as well as the RoHS guidelines and are certified according to DIN EN ISO 9001. Production parameters, production conditions and raw materials are assessed and registered using calibrated measuring instruments.

The printed circuit boards are subjected to the following tests during the production process to ensure perfect quality:

Non-destructive testing

For automatic and optical tests, we adhere to the IPC-A 600, Class 2 guideline. Specific test procedures can also be adapted to other specifications at any time if required.

Destructive testing

- Micrograph creation,
- Adhesion test,
- Delamination test (multilayers are regularly subjected to thermal shock tests).

Documentation of the parameters

Automatic recording and storage of the following parameters for at least 10 years:

- Production parameters,
- quality-related results,
- Time recording, including the respective employees.

X-Ray

X-ray fluorescence spectrometry for layer registration and layer thickness measurement.

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5. Electrical testing

During the final electrical test, circuit boards are checked for open circuits and short circuits.

The client's Gerber data is loaded into our test system, from which a netlist is generated containing all the test points identified. These test systems test according to the following criteria as standard:

- for interruption if > 10 Ohm network resistance is detected
- to close if resistances < 10 MegOhm are detected between independent shunts

We use the following test systems:

5.1 Test adapter/parallel tester

Based on the test programme, adapter plates are drilled and fitted with test needles, which are deflected to the relevant contact points in order to simultaneously record all end points of the electronic network for the test procedure for short circuit and open circuit. At the same time, all networks are tested against each other. The test result is then compared with the electrical network list.

5.2 Finger tester (Flying Probe)

Alternatively, the electrical test can be carried out using a finger tester. The contact points of the circuit board are contacted sequentially with contact needles using the underlying netlist and tested for short circuits and interruptions. Measuring needles are suspended from mechanically movable "fingers", which move to the previously programmed test positions.

In all test procedures, the PCBs on which a short circuit or an open circuit was detected are automatically separated from the PCBs that were clearly tested without faults. A fault log with the exact fault position is created for faulty or not clearly tested PCBs. Once the fault has been successfully rectified, the PCB is subjected to a complete test run again.

6. Base material

The CAF (Conductive Anodic Filament) resistant FR4 base material is permanently in our stock.

- in thicknesses from 0.5 to 3.2 mm
- Creepage resistance values (CTI) up to 600 volts
- TG value up to 170 degrees Celsius

Directly available:

- **FR4 TG 135°-140°; CTI 175-249 (standard)**
- FR4 TG 150°
- FR4 TG 170°
- FR4 CTI 250-399 PLC 2
- FR4 CTI 400-599 PLC 1
- FR4 CTI ≥ 600 PLC 0
- CEM1
- CEM3

We also procure other base materials of various thicknesses on request.

6.1 Material properties

The following values apply to a material thickness from 0.5 mm:

Laminate	NEMA	IPC-4101	Tg C°	CTE < Tg ppm/K	CTE > Tg ppm/K	Decomposition temperature C°	T260 min	T288 min	
epoxy-paper-glass	**CEM1**	10	100	-	-	-			
epoxy-glass	**FR4.0**	21	135	70	280	310	20	2	**Standard**
epoxy-glass	**FR4.0**	99	150	60	250	350	60	20	**high Tg inorganic fillers**
epoxy-glass	**FR4.0**	101	170	60	230	350	60	20	**higher Tg inorganic fillers**
epoxy-glass	**FR4.1**	128	150	50	230	340	60	20	**halogen-free inorganic fillers**
epoxy-glass	**FR4.1**	130	170	50	230	350	60	20	**higher Tg halogen-free inorganic fillers**

6.2 Copper foil thickness standard (before galvanic copper plating)

18 µ	35 µ	50 µ	70 µ	85 µ	105 µ

6.3 Copper-clad laminates

<table>
<tr><th colspan="2">FR4 in mm</th><th>FR4 CTI > 400</th><th>CEM 1
(on request)</th><th>CEM 3
(on request)</th></tr>
<tr><td>0,10</td><td>plus Cu</td><td rowspan="6">1,00</td><td rowspan="6">1,00</td><td rowspan="13">1,55</td></tr>
<tr><td>0,20</td><td>plus Cu</td></tr>
<tr><td>0,25</td><td>plus Cu</td></tr>
<tr><td>0,36</td><td>plus Cu</td></tr>
<tr><td>0,41</td><td>plus Cu</td></tr>
<tr><td>0,50</td><td>plus Cu</td></tr>
<tr><td>0,71</td><td>plus Cu</td><td rowspan="7">1,55</td><td rowspan="7">1,55</td></tr>
<tr><td>1,00</td><td>incl. Cu</td></tr>
<tr><td>1,08</td><td>plus Cu</td></tr>
<tr><td>1,55</td><td>incl. Cu</td></tr>
<tr><td>2,00</td><td>incl. Cu</td></tr>
<tr><td>2,40</td><td>incl. Cu</td></tr>
<tr><td>3,00</td><td>incl. Cu</td></tr>
</table>

7. Tolerances for twisting and warping

One-sided	Double-sided	Multilayer
1,5 %	1 %	1 %

Please note that the warping value increases above average if the copper distribution on the PCB is very different locally. Especially with multilayers, a symmetrical layer structure should be planned right at the start of layout development. Asymmetrical material structures can result in higher twisting and warping values due to the different tensions of the glass fibre qualities.

8. Available production benefits

In order to manufacture economically and sustainably, we check the best possible utilisation of our production capacity and compare this with the most frequently used PCB sizes to avoid unnecessary waste.

	Single-sided printed circuit boards mm		Double-sided printed circuit boards mm		4-ply LP standard construction MassLam mm		4-layer LP with over 6 prepregs and 6-24 layers of LP PinLam mm	
	Length	Width	Length	Width	Length	Width	Length	Width
Panel size 1	618	512	614	512	614	512	600	499
Panel size 2	Not available		584	512	584	512	Not available	
Panel size 3	584	436	Not available		Not available		Not available	

9. Circuit board thickness

We can process different PCB thicknesses regardless of the number of layers.

Lead times for special material thicknesses may vary if the required material is not in stock.

	Standard mm	Special mm	Technical limit Single and double-sided mm	Technical limit Multilayer mm
Min. panel thickness	1,55	0,8	0,4	0,4
Max. panel thickness	1,55	2,4	3,2	3,2

10. Multilayer plies and superstructures

Multilayers consist of copper layers, prepregs and thin laminates. These can be combined in completely different ways, resulting in an infinite variety of construction options. We manufacture multilayers with up to 24 layers. The layers can then be connected to each other via vias between the outer layers (vias), from an outer layer to an inner layer (blind vias or blind holes) or between the inner layers (buried vias).

The most frequently used layer structures can be found on our website in the Download Centre.

Of course, you can also contact our sales team directly if you have any questions. We will be happy to send you special layer structures on request.

The following basic principles should be observed when creating a multilayer layout:

10.1 Symmetry

Right from the initial design, a symmetrical material structure should be planned that takes into account identical thin laminates and prepreg types in the same order. This significantly reduces twisting and warping (stresses released by thermal and mechanical effects during the machining process and use), among other things.

10.2 Consideration of physical influencing variables

For some special designs, the material structure (stack-up) of a multilayer is particularly decisive. Which layer structure should be selected depends on various physical factors.

The most important parameters are

- Dielectric strength of the layers to each other
- Permittivity ε (dielectric conductivity) / "Dk" of the base material (also dielectric constant) with dissipation factor "Df"
- Temperature and moisture content

Dielectric strength

For FR4 base material of 0.5 mm, laminate manufacturers specify a dielectric strength of 800 V - 1200 V/25 µ. However, practice shows that the actual remaining insulation layer between the layers is lower, as prepregs embed themselves in the copper structures during pressing. Thin laminates are recommended as their change in thickness after pressing is negligible.

> Please note that the test methods for determining dielectric strength in accordance with the IPC standard relate to unlaminated materials. The dielectric strength of a complete multilayer is not taken into account. We therefore recommend a sufficient safety margin.

> When starting to design the layout of your multilayer, we advise you to follow the provisions of the IEC, VDE and UL® standards, which contain specifications for sufficient insulation between neighbouring conductors.

Permittivity ε

The thickness and quality of the dielectric (prepreg) between the copper layers influence the capacitance and impedance of the PCB.

Physical values of the common FR4 prepregs:

Prepreg type	Thickness in µ (before pressing)	Thickness in µ (after pressing)	Resin content	Tolerance in %	1 MHz		1 GHz		5 GHz		10 GHz	
					Dk	Df	Dk	Df	Dk	Df	Dk	Df
1080	approx. 75	approx. 70	Ø62 %	+/- 3	3,90	0,017	3,76	0,019	3,72	0,020	3,69	0,020
2116	approx. 120	approx. 115	Ø50 %	+/- 3	4,30	0,016	4,18	0,018	4,15	0,019	4,12	0,019
7628	approx. 190	approx. 180	Ø43 %	+/- 3	4,60	0,017	4,36	0,018	4,34	0,019	4,31	0,019

Physical values of common FR4 thin laminates:

Number of prepregs	Thickness in µ	Resin content	Tolerance in µ	1 MHz		1 GHz		5 GHz		10 GHz	
				Dk	Df	Dk	Df	Dk	Df	Dk	Df
1 x 2116	110	Ø44,5 %	+/- 18	3,93	0,020	4,11	0,017	4,03	0,018	3,97	0,018
1 x 7628	200	Ø44,0 %	+/- 25	4,13	0,019	4,12	0,017	3,96	0,018	3,98	0,018
2 x 7628	360	Ø39,5 %	+/- 38	4,70	0,017	4,21	0,017	4,05	0,018	4,09	0,018

Number of prepregs	Thickness in µ	Resin content	Tolerance in µ	1 MHz		1 GHz		5 GHz		10 GHz	
				Dk	Df	Dk	Df	Dk	Df	Dk	Df
2 x 7628	410	Ø42,5 %	+/- 38	4,40	0,019	4,12	0,017	3,96	0,018	3,98	0,018
3 x 7628	500	Ø39,5 %	+/- 50	4,70	0,017	4,25	0,017	4,10	0,018	4,14	0,018
4 x 7628	710	Ø39,0 %	+/- 50	4,70	0,017	4,25	0,018	4,10	0,019	4,14	0,019

Temperature and moisture content

Please allow for the following tolerances:

- The Dk value increases by approx. 17% after moisture absorption for typical standard FR4.
- The Df value increases by approx. 12% after moisture absorption for typical standard FR4.

Note that thermal stress, such as soldering and thermal cycling, which the PCB experiences during manufacture and use, can also have an effect on the electrical and mechanical properties of the material. Increased temperature leads to thermal expansion, which can result in mechanical stresses and potential defects such as delamination or microcracks. These effects can affect the reliability and longevity of the PCB. Therefore, the thermal stresses to which the PCB will be exposed during use should also be taken into account when planning the multilayer structure.

A well-thought-out layer structure and the choice of suitable materials can help to minimise thermal stresses and extend the service life of the PCB:

- **High-temperature resistant materials:** High-quality prepregs and laminates from the best manufacturers are better able to withstand thermal loads.
- **Reinforced prepregs:** Prepregs with a high glass content offer better mechanical properties and greater thermal stability.
- **Symmetrical structure:** A symmetrical layer structure helps to distribute mechanical stresses evenly and minimise torsion.
- **Optimised layer thicknesses:** Plan the thicknesses of the prepregs and laminates in such a way that thermal expansion is minimised.
- **Sufficient spacing:** Ensure that there is sufficient space between the copper layers to absorb thermal expansion and prevent delamination.

By carefully considering these factors, you can significantly improve the performance and durability of your multilayer PCBs.

If you have any further questions, please contact our sales department or our work preparation department. They can also provide you with samples of layer structures.

11. Ladder diagram creation

The lithographic limit for the resolution of printed circuit boards (track/gap) in the exposure systems we use is the thickness of the dry resist to be exposed. If this has a thickness of 50 µ, the maximum possible resolution is also 50 µ. Physical processes in the subsequent electroplating and etching processes also have a limiting effect. The higher the final copper thickness, the higher the degree of under-etching on the flanks, which must be compensated for in the exposure parameters.

In principle, the reproducibility of a layout depends on the design of the layout and the thickness of the copper structure. The technical restrictions of solder resist production must also be taken into account. When creating and processing the layout, it is necessary to consider the overlap, underlap or even clearance of the conductor flanks and insulation surfaces.

Final copper thickness 35 µ	Standard µ		Special µ		Technical limit µ	
	Outer layers	Inner layers	Outer layers	Inner layers	Outer layers	Inner layers
Conductor width	120	120	100	100	60	60
Conductor spacing	120	120	100	100	70	70
Restring	125	150	100	120	70	80
Registration accuracy	+/- 50 µ		+/- 40 µ		+/- 30 µ	
Final copper thickness 70 µ	**Standard µ**		**Special µ**		**Technical limit µ**	
	Outer layers	Inner layers	Outer layers	Inner layers	Outer layers	Inner layers
Conductor width	150	150	125	125	100	100
Conductor spacing	170	170	140	140	120	120
Restring	180	200	150	170	120	120
Registration accuracy	+/- 50 µ		+/- 40 µ		+/- 30 µ	
Final copper thickness 105 µ	**Standard µ**		**Special µ**		**Technical limit µ**	
	Outer layers	Inner layers	Outer layers	Inner layers	Outer layers	Inner layers
Conductor width	200	200	170	170	130	130
Conductor spacing	250	250	225	225	200	200
Restring	250	275	200	225	150	175
Registration accuracy	+/- 50 µ		+/- 40 µ		+/- 30 µ	
Final copper thickness 140 µ	**Standard µ**		**Special µ**		**Technical limit µ**	
	Outer layers	Inner layers	Outer layers	Inner layers	Outer layers	Inner layers
Conductor width	300	300	250	250	230	230
Conductor spacing	400	400	360	360	320	320
Restring	300	300	270	270	250	250
Registration accuracy	+/- 50 µ		+/- 40 µ		+/- 30 µ	

12. Solder mask

In the photo-technical solder resist process, the surface is embedded in a photosensitive polymer. The chemical cross-linking of the polymers is achieved through the defined exposure; all unexposed zones are developed with sharp contours even in the micrometre range. In order to achieve the required electro-physical properties of the coating, a UV bump, a kind of "vitrification" of the coating surface to reduce ionic contamination, and final thermal curing are then carried out.

With the solder resist coating, the soldering eyes of the via holes can be printed closed on request. However, this does not guarantee that the VIA holes are sealed (via plugging) (unsuitable for vacuum testers).

However, if it is absolutely necessary to seal the vias, this process is carried out in a separate procedure in which the holes in question are specially coated with lacquer and sealed.

Up to a hole diameter of 0.45 mm, sealing is possible with standard varnishes. For larger hole diameters, a special varnish or resin filling is required.

12.1 Solder resist parameters

We only use epoxy resin-based solder resists, as these also improve the tracking resistance on the surface of the PCBs.

Values apply to green solder resist	Standard µ	Special µ	Technical limit µ
Circumferential expansion of the solder mask	70	50	30
Minimum web width	80	60	50
Min. distance SMD to SMD*	200	170	150
Registration accuracy	+/- 40 µ	+/- 35 µ	+/- 30 µ

*Minimum distance between solder resist-free surfaces in order to be able to reproduce a solder resist bridge

When creating solder-stop masks, solder-stop clearances in a ratio of 1:1 to the pads, i.e. without oversizing, must be taken into account. We calculate the expansion required for production ourselves.

The following solder resist colours are possible:

- **green (standard)**
- blue
- black
- red
- white

TOP/BOTTOM can be painted in different colours.

13. Galvanic copper deposition process

The thickness of the copper plating depends on the exposure time and the current in the electroplating bath.

In principle, a deposition of 20 µ to 25 µ copper is applied to the surface and in the holes to be plated through during the process. Thicker copper layers are possible by adjusting the process parameters or additional galvanic processes.

In order to achieve uniform copper deposition, the layout design should take into account that trace structures are either not embedded in ground or completely embedded in ground. The conductor tracks or pad positions should be centred within a ground embedding and at equal distances from each other. If copper structures are unevenly distributed in the layout, there is a tendency towards over-deposition in the "low-mass" regions. This leads to a reduction in the track spacing and even to electrical failure due to a short circuit, as the tracks literally grow together.

Copper foil µ	Electrolytic copper deposition	Final copper thickness
18 µ	approx. 20 µ	approx. 35 µ
35 µ		approx. 55 µ
50 µ		approx. 70 µ
70 µ		approx. 90 µ
85 µ		approx. 105 µ
105 µ		approx. 125 µ

13.1 Aspect ratio

The "aspect ratio" defines the ratio of "material thickness to hole diameter".

It is determined as follows: Material thickness divided by the smallest hole diameter.

Example: *1.6 mm material thickness divided by 0.2 mm hole diameter = 8*

The efficiency of electrolytic copper deposition is expressed in the aspect ratio, the ratio of the diameter of a hole to the contactable depth of this hole.

Standard	Special	Technical limit
6	8	10

This value is very important for the manufacturability of the PCB, because the higher the aspect ratio, the more complex it is to produce metallisation in the holes.

13.2 Microfilling (via-in-pad)

This technology enables the simultaneous filling of blind vias and the reinforcement of through-holes.

With HDI circuits, there is usually not enough space to route the signals to different layers using through-holes. A space-saving solution is to position blind vias in SMD pads that are filled with copper after drilling. Due to this filling, only a very small amount of solder flows into the remaining "surface dent" (dimple) and enables a solder joint as intended. The maximum drilling diameter and the maximum drilling depth is 0.15 mm.

13.3 Via plugging via resin filling (also suitable for via-in-pad technology)

Sealing both continuous and blind vias with resin combined with subsequent metallisation is an alternative to microfilling, but this method is more complex in terms of process technology.

The advantages over microfilling are that

- continuous holes from 0.1 mm to 2 mm can also be sealed; however, the material thickness must not be smaller than the hole diameter.
- a planar sealing of the holes is possible; no dimple remains in the pad.

14. Surface finishing

We can currently realise the following end surfaces for you:

- Hot air tinning lead-free (HAL) - Sn / 0.3 Ag / 0.7 Cu / 0.02 Ni
- Electroless nickel-gold (ENIG) - 99.9 Au
- Electroless nickel-palladium-gold (ENEPIG)
- Chemical tin (chem. Sn)
- Chemical silver (chem. Ag)
- Organic tarnish protection (OSP)
- Electroplated nickel-gold (hard and bond gold) - hard 99.8 Au / soft 99.99 Au

Properties of the various end surfaces:

	HAL	ENIG	ENEPIG	chem. Sn	chem. Ag	OSP	Galvanised Au
Layer thickness µ	<10	0.05-0.12 Au 4-8 Ni	0.03-0.10 Au 3-7 Ni 0.08-0.30 Pd	0,80-1,20	0,15-0,45	0,02-0,06	0,80-5,00
Planarity	+	+++	+++	+++	+++	+++	+++
Shelf life with stable conditions	<12 months	<12 months	<12 months	<6 months	<6 months	<6 months	<12 months
Multiple solderability	+++	+++	+++	+	++	o	yes (soft)
Reactivatable	Yes	conditional	conditional	Yes	Yes	Yes	no
Aluminium wire bonding	no	Yes	Yes	no	conditional	no	yes (soft)
Au wire bonding	no	no	no	no	no	no	yes (soft)
Pushbutton contact	no	Yes	Yes	no	no	no	Yes
Press-fit technology	Yes	no	no	Yes	Yes	no	no

15. Printing techniques

15.1 Serialisation

In order to ensure that PCBs can be clearly identified, individualised marking of the individual PCBs can also be selected within a series. This marking is applied automatically (direct exposure of the structures or placement printing) in white colour and can consist of static information (e.g. production dating, date code, etc.) and consecutive numbering in chronological order and can be displayed in the following machine-readable formats:

- **1D & 2D barcodes, Data Matrix, QR codes.**

15.2 Labelling print / placement print

To avoid interruptions or blurring within the typeface, the line width of the marking print should not be less than 130 µ and the font height should not be less than 1000 µ. The soldering surfaces should be kept free from the marking print by at least 250 µ all the way round, as otherwise an unclean print image and pressure on the soldering surfaces is possible.

	Standard µ	Special µ	Technical limit µ
Distance print image to pad	200	150	100
Distance print image to holes	200	150	100
Line width	130	100	75
Font size	1000	750	500
Registration accuracy	+/- 200 µ	+/- 150 µ	+/- 70 µ

15.3 Carbon printing

	Standard µ	Special µ	Technical limit µ
Distance between the carbon surfaces	500	400	300
Minimum width of the carbon surface	700	600	500
Registration accuracy	+/- 250 µ	+/- 200 µ	+/- 150 µ

15.4 Stripping varnish

The layer thickness of the strippable coating is approx. 500 µ.

Holes that are covered with strippable paint should not exceed a size of 1.8 mm.

	Standard	Special	Technical limit
Maximum spanable diameter	1.8 mm	2.0 mm	2.6 mm*
Minimum width	6 mm	5 mm	4 mm
Registration accuracy	+/- 300 µ	+/- 250 µ	+/- 200 µ

*Complete covering of the hole cannot be guaranteed.

16. Contour machining

We drill, mill and score your PCBs according to your specifications and wishes. The type of mechanical processing depends on your individual specifications. In our drilling and milling centre, we work with modern, fully automatic CNC drilling and milling machines. These techniques enable machining within the DIN 7168 standard "medium" (medium accuracy) and "fine" (precise accuracy).

If non-plated-through holes are positioned in a soldering eyelet, this must be at least 500 µ larger all round than the hole. Otherwise, solder eyes may be removed.

If there is no information on the type of drill holes for plated-through PCBs, we determine to the best of our knowledge which holes are plated through and which are not.

If drilling or dimensional plans are provided which do not correspond to the drilling programmes or the contour according to the layout data, the drilling programmes and the contour according to the layout data are binding for production in all cases.

Unless otherwise specified, the centre point (= centre vector) of the contour lines in the layout data is decisive for the contour of the PCB. If slots are represented by rectangular contours, we assume that the corner radius is included.

Depending on the size of the printed circuit boards, the following tolerances are specified (other tolerance values are possible by agreement):

Format mm	Medium mm	Fine mm
0,5-6	+/- 0,10	+/- 0,05
6-30	+/- 0,20	+/- 0,10
30-120	+/- 0,30	+/- 0,15
120-400	+/- 0,50	+/- 0,20
400-1.000	+/- 0,80	+/- 0,30

16.1 Scoring (notch milling)

The angle of the scribing blades is 15°. Therefore, along the contours that are scribed, a distance between the conductor tracks and the contour must be taken into account in accordance with the following table:

Material thickness mm	Distance between conductor tracks and contour mm
up to 1.00	0,45
1,10 - 1,60	0,50
1,70 - 2,00	0,70
2,10 - 2,50	0,80
2,60 - 3,20	1,00

If no plus tolerance is permitted for the contour, the desired minus tolerance must be added to the "Distance of conductor tracks to contour" values specified above.

Example: PCB format 100 mm x 100 mm +0.00/-0.30 mm

Distance between conductor tracks and contour with 1.6 mm material thickness: 0.5 mm + 0.15 mm = 0.65 mm

16.2 Milling

As an alternative to scoring, we offer contour milling. The advantage over scoring is that the outer contours can be machined in the most specialised shapes and cut-outs, such as round, oval, wavy, zigzag, etc.

Please note when milling:

- If delivery is to take place in the routing panel, a distance of 2.0 mm between the PCBs is sufficient as standard in order to be able to place routing bridges between the individual PCBs.
- If the delivery is not to be made in a panel, a distance of at least 8.0 mm from board to board must be taken into account in order to be able to separate the PCBs in the end.

16.3 Deep milling and drilling / countersink drilling

Milling and drilling with a defined Z-axis is carried out according to your drawing specifications. Countersinks are produced at 45° or 30° as standard. The specifications for this can be customised.

16.4 Milling and scoring combination

In some cases, it makes sense to combine both milling and scribing in order to achieve the best compromise between cost and material loss. Our CNC machines are able to realise these combinations precisely.

16.5 Chamfering

For easier installation of plug contacts (e.g. PCI connectors), edge bevelling at 45° or 30° at different depths is possible.

16.6 Edge metallisation

To realise edge contacts, we can produce special edge metallisation (e.g. side plating or castellated holes). This is particularly useful when improved electrical conductivity or shielding is required.

16.7 Semiflex

In semi-flex technology, a defined area of rigid PCBs is milled down to a residual material thickness in order to be able to bend the material there. Although the same bending angles and radii cannot be realised in comparison to rigid-flex circuits / rigid-flex, they are often sufficient for the applications. Depending on the design, semiflex technology allows three to five bends; the PCB must therefore be mounted statically.

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The main advantages lie in the more favourable production process and the elimination of the otherwise necessary polyimide film, which in turn would require thermal pre-treatment due to the high moisture absorption.

17. Drilling and milling tolerances

Plated-through holes (PTH)		Standard mm	Special mm	Technical limit mm
Smallest drilling diameter		0,35	0,15	0,10
Largest drilling diameter		6,00	6,00	6,00
Smallest distance between borehole tangents*		0,20	0,15	0,075
Smallest distance between hole bar centre and conductor track*	Outer layers	0,20	0,15	0,075
	Inner layers	0,25	0,20	0,10
Surface Hot air levelling Tin plating Tolerance	Final diameter <= 6 mm	+0,10/-0,05	+0,09/-0,06	+0,08/-0,05
	End diameter > 6 mm milled	+0,14/-0,05	+0,10/-0,05	+0,08/-0,05
Surface OSP/ENIG/chemical tin/silver Tolerance	Final diameter <= 6 mm	+0,10	+0,05/-0,05	+0,10
	End diameter > 6 mm milled	+0,12/-0,02	+0,06/-0,06	+0,10

Hole position tolerance of plated-through holes to non-plated-through holes and to the contour	+/-0,20	+/-0,07 **	+/-0,05 ***

Non-plated through holes (NPTH)		Standard mm	Special mm	Technical limit mm
Smallest drilling diameter		0,40	0,20	0,15
Largest drilling diameter		6,40	6,40	6,40
Smallest distance between borehole tangents*		0,20	0,15	0,10
Smallest distance between hole bar centre and conductor track*	Outer layers	0,20	0,15	0,05
	Inner layers	0,25	0,20	0,10
Tolerance	Final diameter <= 2 mm	+/-0,05	+/-0,03	+/-0,03
	End diameter 2 <= 6 mm	+0,1/-0,05	+/-0,05	+/-0,03
	End diameter > 6 mm milled	+0,1/-0,05	+/-0,06	+/-0,04

*Please note that plated-through holes generally have to be drilled or milled 150 µ larger than the desired final diameter in order to compensate for the metallisation in the hole. For example, if you want a final diameter of 0.6 mm, the diameter of the drill used is 0.75 mm, unless deviating tolerances are specified.

**depending on the hole diameter

***provided that the drilling process is carried out in a machine clamping (tenting)

18. Storage

18.1 Humidity

Due to the epoxy resin in the base material of the printed circuit boards, they (especially multilayers) are extremely hydrophilic, i.e. the water molecule dissolved in the air is absorbed by the material. Depending on the ambient conditions, moisture equilibrium is established in materials. Under storage conditions of 20 degrees Celsius and 35 per cent humidity, for example, moisture absorption of 0.12 per cent (in per cent by weight of the epoxy resin) can be observed after just 12 days. The decisive factor here is that the higher the moisture absorption, the higher the gas pressure inside the PCB, which is caused by the high temperatures during the soldering process. If the moisture absorption exceeds 0.17 per cent, a critical gas pressure of 8 - 10 bar is reached, at which delamination and blistering can occur. Epoxy resin can absorb up to 0.5 per cent moisture by weight.

To ensure that the moisture content and the adhesive bond of the material are perfect, we carry out a delamination test using a test specimen after the multilayer printed circuit boards have been completed.

To further prevent or reduce moisture absorption, we strongly recommend the following points:

Storage environment

PCBs should be stored in a constantly heated environment under controlled conditions, preferably in darkened rooms, until shortly before soldering/processing. Due to climatic changes, a controlled storage environment is becoming increasingly important in order to maintain the quality of the PCBs. Humidity and temperature fluctuations should be minimised and the packaging of the PCBs should be checked for integrity before processing.

We strongly recommend that you maintain the following conditions in the storage environment in order to minimise moisture absorption:

- Room temperature 18- 21 °C
- Relative humidity < 50 %

Packaging

Preferably store in closed containers. We would like to point out that polyethylene bags do not provide reliable protection against moisture due to their water vapour permeability. To improve protection, we therefore also offer to pack the PCBs in DRY-SHIELD protective bags. They can also be vacuum-packed and/or provided with indicator and dry bags. The protective films/bags should only be removed shortly before soldering/processing. We recommend that residual quantities be vacuum-sealed again, or at least securely sealed with adhesive tape or by clamping the film between the PCBs and stored in boxes to prevent draughts.

Storage time

The storage time of PCBs should be as short as possible and consumption should follow the "first-in, first-out" rule. For storage times of more than 3 months (based on the production period), it is difficult to predict when moisture absorption may lead to problems during soldering/processing due to a wide variety of influencing parameters such as layout, layer structure, etc. For reliable proof of the storage time, we can apply a production date / date code to the PCBs by agreement. Please note that the shelf life also depends on the selected final surface. You will find orientation values for this in the Surface finishing section of this document. Please always consume opened packages first.

18.2 Soldering test

PCBs that have already been stored for several months and whose transport conditions are unclear (transport of goods by haulage companies in all weathers and temperatures) should definitely be subjected to a soldering test before further processing.

18.3 Preconditioning/drying

In order to reduce the absorbed moisture, we recommend drying the goods in an oven, irrespective of the outcome of a soldering test, whereby the PCBs should preferably be dried vertically in a rack. If you store the PCBs with us for more than four months (e.g. when ordering on call), we will dry them before delivery in any case.

Degree °C	Drying time
120	4 hours
110	6 hours
100	8 hours

If drying in a vacuum oven at 50 mbar is possible, the temperature can be reduced by approx. 20 °C and the time by approx. 30 minutes. This procedure is advantageous for the sensitive "chemical tin" surface. A few test specimens should then be used to determine whether the solder still wets sufficiently; otherwise, the immersion tin must be refreshed.

After drying, processing of the PCBs should begin immediately, as the hydrophilic properties of the PCB remain. The time between the various soldering processes must be kept as short as possible and should not exceed 8 hours. This is the only way to avoid excessive moisture absorption in unprotected material. Dried and tempered PCBs will become saturated with water from the ambient air for a short time.

18.4 Product-specific requirements

The values stated in the previous sections are approximate values.

The values do not conclusively take into account the different processing parameters and product-specific properties of the individual PCBs and must be determined by the respective processor on a product-specific basis:

- The different soldering processes and profiles cause different loads. For example, the thermal load in convection ovens is not as high as in infrared ovens or vapour phases.
- If the recommended storage conditions cannot be maintained at all times, the material will absorb more water than is possible under constant conditions. Packaging in DRY-SHIELD protective bags can help here.
- If the layout contains large, closed copper surfaces, the moisture will take longer to escape.
- the multilayer structure. see: 10.2 Consideration of physical influencing variables