Technical delivery terms (TLB), recommendations and design rules for printed circuit boards

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Precoplat GmbH – Printed circuit boards made in Germany

Precoplat Präzisions-Leiterplatten-Technik GmbH is one of the leading printed circuit board manufacturers in Germany. As a medium-sized family-run business, we have been manufacturing unassembled printed circuit boards at our production site in Krefeld, North Rhine-Westphalia, since the 1970s. 100% Made in Germany.

On our premises, which cover around 25,000 m², over 70 employees use highly technical and automated processes to produce more than 100,000 m² of printed circuit boards annually. We supply a wide range of industries internationally and can respond quickly and flexibly to customer requirements.

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1. Products

Our product range includes single-sided PCBs, double-sided PCBs and through-hole PCBs, multilayer PCBs with up to 24 layers, as well as semi-rigid PCBs, from prototypes to (large-scale) series production. Our processes are designed to ensure the highest quality and reliability. **PRECOPLAT is your expert PCB manufacturer in Germany.**

For medium and large production runs of up to 25 m² per order, we offer an express service, which can be implemented as follows:

Type	Express	Average processing time
Standard* single- and double-sided LP	3 days	~ 12 days
Standard* multilayer	4 days	~ 15 days

*Standard: 1–4-layer PCB using hot air levelling technology, solder mask, FR4 material, conventional drilling techniques

Our service begins with technical support and extends through to integration into our customers' supply chain management. In doing so, we take every unique specification and individual requirement into account.

We always distinguish between three service categories: Standard, Special and Technical Limit.

2. Data

2. Data

Our CAM staff ensure the implementation of your layouts right through to the finished PCB.

If you are unable to generate the files in the formats described, please contact our sales team.

You can send us your production data in the following formats:

2.1. Layout data

- Extended Gerber 274x (standard)
- Gerber 274
- Eagle
- Autodesk Fusion 360
- ODB++

2.2. Drilling and milling data

- Excellon (Standard)
- Drillfile in Sieb & Meyer Format 3000

Mechanical drawings can also be submitted in HPGL or DXF format.

3. Design Rule Check

3. Design Rule Check

All data supplied to us is checked for manufacturability using a standard Design Rule Check in accordance with IPC-2211, as well as customer-specific DFM functions. We handle vias and their protection or closure types in accordance with IPC-4761 as standard. An overview of our processes (tenting, plugging, filling & capping) can be found in Chapter 10.

Additional services (e.g. impedance control, layout/data modifications, reverse engineering) are provided on request and exclusively following a separate order.

3.1. HDI/Micro-Vias

For micro-vias (HDI), we adhere to **IPC-2221 / IPC-2226** and the **ZVEI design guidelines**. The following guidelines apply to the design rule check:

- Restring on micro-vias: ≥ 100 µm (standard), ≥ 75 µm (special).
- Aspect ratio of micro-vias (drill depth ÷ hole diameter): ≤ 1 : 1.
  Example: Hole Ø 100 µm, drilling depth 63 µm → AR = 0.63 : 1.

Note: Copper foil thickness in accordance with 6.2. Standard copper foil thickness (prior to electroplating); deviations are possible subject to prior agreement. For BGA / CSP / Flip-Chip / COF, we take this into account in the design rule check and data verification (including pad geometry, via-in-pad, restricting, solder mask, clearances).

3.2. Optional engineering services

Software-assisted impedance control (= in-depth control): Creation of a Polar report (calculation/validation) based on the approved layer stack-up; target values and tolerances as specified by the customer.

Reverse engineering (scanning of submitted PCBs): Recording of the layer stack-up, capture of trace patterns/drill data/net information and reconstruction of CAM-compatible manufacturing data (e.g. Gerber/ODB++); implementation only subject to usage rights clarified by the client.

4. Quality

4.1. Quality standards

We manufacture **unassembled printed circuit boards in accordance with IPC-6012 (including Addendum – Space and Military / Medical (on request)), Class 2 or Class 3. Acceptance is carried out in accordance with IPC-A-600, Class 2 or Class 3.**

In addition, we support the following standards/specifications on request:

- Solder resist (material/qualification): **IPC-SM-840**
- Finish (ENIG): **IPC-4552**
- Design principles (customer layout): **IPC-2221**
- Via protection types (filling & capping): **IPC-4761**
- HDI/Micro-Vias Design (customer layout): **IPC-2226**
- **PERFAG** (European specification for supply agreements & quality levels)
  - PERFAG 1 – single-sided
  - PERFAG 2 – double-sided
  - PERFAG 3 – Multilayer
- **Railway applications:** Test reports in accordance with **EN 45545-2** can be provided for suitable material systems.
- **Semiflex** (thinned FR4, 'flex-to-install'): Manufactured as a rigid printed circuit board in accordance with IPC-6012; inspected in accordance with IPC-A-600; not an IPC-6013 product.

The revision valid at the date of order confirmation applies in each case.

4.2. Quality assurance

We comply with UL® standards and the RoHS directives and are certified to DIN EN ISO 9001. Production parameters, production conditions and raw materials are assessed and recorded using calibrated measuring instruments.

During the production process, the printed circuit boards are subjected to the following tests to ensure flawless quality:

Non-destructive testing

For visual inspections, we use IPC-A-600 as an image reference; acceptance is based on the ordered class (Class 2/3). AOI minimum structure: 25 µ. Specific test procedures can also be adapted to other specifications at any time if required.

Destructive testing

- Cross-section analysis,
- adhesion test,
- delamination test (multilayers are regularly subjected to thermal shock tests).

Documentation of parameters

Automatic recording and storage of the following parameters for at least 10 years:

- Production parameters,
- quality-related results,
- time recording, including the relevant employees.

X-ray

X-ray fluorescence spectrometry for layer registration and coating thickness measurement.

AQAP

AQAP-2110 requirements are implemented internally. For projects subject to AQAP, we plan the official quality assessment (GQA) and apply for BAAINBw certification on a project-by-project basis.

5. Electrical testing

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During the final electrical test, printed circuit boards are checked for open circuits and short circuits.

The client’s Gerber data is loaded into our testing system, from which a netlist is generated containing all identified test points. These test systems test by default according to the following criteria:

- for open circuits, if a network resistance of > 10 ohms is detected
- for short circuits, if resistances < 10 megohms are detected between independent shunts

We use the following test systems:

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5.1. Test adapters/parallel testers

Using the test programme, adapter plates are drilled and fitted with test probes, which are directed to the relevant contact points in order to simultaneously detect shorts and open circuits at all end points of the electronic network during the test process. In parallel, all networks are tested against one another. The test result is then compared with the electrical netlist.

5.2. Flying probe tester

Alternatively, the electrical test can be carried out using a flying probe tester. The contact points on the printed circuit board are sequentially contacted by test probes in accordance with the underlying netlist and tested for continuity and open circuits. In this process, test probes are attached to mechanically movable ‘fingers’ which move to the pre-programmed test positions.

In all test procedures, the printed circuit boards on which a short circuit or an open circuit has been detected are automatically separated from those that have been unequivocally tested as fault-free. For faulty or not unequivocally tested printed circuit boards, a fault report is generated with the exact fault location. Once the fault has been successfully rectified, the printed circuit board is subjected to a full test run again.

6. Base material

6. Base material

The CAF (Conductive Anodic Filament)-resistant FR4 base material is permanently in stock.

- in thicknesses from 0.5 to 3.2 mm
- Creepage current resistance (CTI) up to 600 volts
- TG value up to 180 degrees Celsius

Available immediately:

- **FR4** TG 135°–140°; CTI 175–249 **(standard)**
- FR4 TG 150°
- FR4 TG 180°
- FR4 CTI 250–399 PLC 2
- FR4 CTI 400–599 PLC 1
- FR4 CTI ≥ 600 PLC 0
- CEM1
- CEM3

Test reports in accordance with EN 45545-2 (up to HL3) are available for our FR4 base material for web applications. Thanks to high-quality FR4 grades, a halogen-free FR4.1 material is not always required, depending on the application. We can supply other base materials, such as FR4.1, in various thicknesses on request.

6.1. Material properties

The following values apply to a material thickness of 0.5 mm or more:

Laminate	NEMA	IPC-4101	Tg °C	CTE < Tg ppm/K	CTE > Tg ppm/K	Decomposition temperature °C	T260 min	T288 min	

epoxy-paper-glass	**CEM1**	10	100	-	-	-			
epoxy-glass	**FR4.0**	21	135	70	280	310	20	2	**Standard**
epoxy-glass	**FR4.0**	99	150	60	250	350	60	20	**High Tg inorganic fillers**
epoxy-glass	**FR4.0**	101	170	60	230	350	60	20	**Higher Tg inorganic fillers**
epoxy-glass	**FR4.1**	128	150	50	230	340	60	20	**halogen-free inorganic fillers**
epoxy-glass	**FR4.1**	130	170	50	230	350	60	20	**Higher Tg Halogen-free inorganic fillers**

6.2. Standard copper foil thickness (prior to electroplating)

18 µ	35 µ	50 µ	70 µ	85 µ	105 µ

6.3. Copper-clad laminates

<table>
<tr><th colspan="2">FR4 in mm</th><th>FR4 CTI > 400</th><th>CEM 1
(on request)</th><th>CEM 3
(on request)</th></tr>
<tr><td>0.10</td><td>plus Cu</td><td rowspan="6">1.00</td><td rowspan="6">1.00</td><td rowspan="13">1.55</td></tr>
<tr><td>0.20</td><td>plus Cu</td></tr>
<tr><td>0.25</td><td>plus Cu</td></tr>
<tr><td>0.36</td><td>plus Cu</td></tr>
<tr><td>0.41</td><td>plus Cu</td></tr>
<tr><td>0.50</td><td>plus Cu</td></tr>
<tr><td>0.71</td><td>plus Cu</td><td rowspan="7">1.55</td><td rowspan="7">1.55</td></tr>
<tr><td>1.00</td><td>incl. Cu</td></tr>
<tr><td>1.08</td><td>excl. Cu</td></tr>
<tr><td>1.55</td><td>incl. Cu</td></tr>
<tr><td>2.00</td><td>incl. Cu</td></tr>
<tr><td>2.40</td><td>incl. Cu</td></tr>
<tr><td>3.00</td><td>incl. Cu</td></tr>
</table>

7. Tolerances for twisting and warping

Single-sided	Double-sided	Multilayer
1.5%	1%	1%

Please note that the warpage value increases disproportionately if the copper distribution on the PCB varies significantly from one area to another. Particularly in the case of multilayer boards, a symmetrical layer structure should be planned right at the start of the layout development. In the case of asymmetrical material structures, higher torsion and warpage values may result from the differing stresses of the glass fabric grades.

8. Available production sheets

To ensure cost-effective and sustainable production, we assess the optimal utilisation of our production sheets and align this with the most commonly used PCB sizes to avoid unnecessary waste.

	Single-sided PCBs mm		Double-sided PCBs mm		4-layer PCB, standard MassLam construction, mm		4-layer PCB with over 6 prepregs and 6–24 layers, PinLam mm	
	Length	Width	Length	Width	Length	Width	Length	Width
Panel size 1	618	512	614	512	614	512	600	499
Panel size 2	Not available		584	512	584	512	Not available	
Panel size 3	584	436	Not available		Not available		Not available	

9. PCB thickness

We can process different PCB thicknesses regardless of the number of layers.

Lead times for special material thicknesses may vary if the required material is not in stock.

	Standard mm	Special mm	Technical limit Single and double-sided mm	Technical limit Multilayer mm
Min. panel thickness	1.55	0.8	0.4	0.4
Max. panel thickness	1.55	2.4	3.2	3.2

10. Multilayer design and via technologies

10. Multilayer Layers and Structures

Multilayers consist of copper layers, prepregs and thin laminates. These can be combined in a wide variety of ways, resulting in an infinite range of configuration options. We manufacture multilayers with up to 24 layers. The layers can then be connected via through-holes between the outer layers (vias), from an outer layer to an inner layer (blind vias or blind holes) or between the inner layers (buried vias).

You can find the most commonly used layer configurations on our website in the Download Centre.

Of course, if you have any questions, please feel free to contact our sales team directly. We will be happy to send you specific layer configurations on request.

The following principles should be observed when creating a multilayer layout:

10.1. Symmetry

A symmetrical material structure should be planned right from the initial design stage, taking into account identical thin laminates and prepreg types in the same sequence. Among other things, this significantly reduces warping and buckling (stresses released by thermal and mechanical effects during the manufacturing process and use).

10.2. Consideration of physical influencing factors

For some specific designs, the material stack-up of a multilayer is particularly crucial. The choice of layer configuration depends on various physical factors.

The most important parameters are:

- Dielectric strength between the layers

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- Permittivity ε (dielectric conductivity) / 'Dk' of the base material (also known as the dielectric constant) with loss factor 'Df'

Dielectric strength

For 0.5 mm FR4 base material, laminate manufacturers specify a dielectric strength of 800 V – 1200 V/25 µ. However, in practice, the actual remaining insulation layer between the layers is found to be thinner, as prepregs embed themselves into the copper structures during pressing. Thin laminates are recommended, as their change in thickness after pressing is negligible.

> Please note that the test procedures for determining dielectric strength in accordance with the IPC standard apply to unlaminated materials. The dielectric strength of a complete multilayer board is not taken into account. We therefore recommend applying a sufficient safety margin.

> When starting the layout design of your multilayer board, we advise you to follow the provisions of the IEC, VDE and UL® standards, which contain specifications for adequate insulation between adjacent conductors.

Permittivity ε

The thickness and quality of the dielectric (prepreg) between the copper layers influence the capacitance and impedance of the printed circuit board.

Physical properties of common FR4 prepregs:

Prepreg type	Thickness in µ (before pressing)	Thickness in µ (after pressing)	Resin content	Tolerance in %	1 MHz		1 GHz		5 GHz		10 GHz	
					Dk	Df	Dk	Df	Dk	Df	Dk	Df
1080	approx. 75	approx. 70	Ø 62%	± 3	3.90	0.017	3.76	0.019	3.72	0.020	3.69	0.020
2116	approx. 120	approx. 115	Ø 50%	± 3	4.30	0.016	4.18	0.018	4.15	0.019	4.12	0.019
7628	approx. 190	approx. 180	Ø 43%	± 3	4.60	0.017	4.36	0.018	4.34	0.019	4.31	0.019

Physical properties of standard FR4 thin laminates:

Number of prepregs	Thickness in µ	Resin content	Tolerance in µ	1 MHz		1 GHz		5 GHz		10 GHz	
				Dk	Df	Dk	Df	Dk	Df	Dk	Df
1 x 2116	110	Ø 44.5 %	+/- 18	3.93	0.020	4.11	0.017	4.03	0.018	3.97	0.018
1 x 7628	200	Ø 44.0 %	± 25	4.13	0.019	4.12	0.017	3.96	0.018	3.98	0.018
2 x 7628	360	Ø 39.5 %	+/- 38	4.70	0.017	4.21	0.017	4.05	0.018	4.09	0.018
2 x 7628	410	Ø 42.5%	+/- 38	4.40	0.019	4.12	0.017	3.96	0.018	3.98	0.018
3 x 7628	500	Ø 39.5 %	± 50	4.70	0.017	4.25	0.017	4.10	0.018	4.14	0.018
4 x 7628	710	Ø 39.0%	+/- 50	4.70	0.017	4.25	0.018	4.10	0.019	4.14	0.019

Temperature and humidity

Please allow for the following tolerances:

- The Dk value increases by approx. 17% following moisture absorption for typical standard FR4.

- The Df value increases by approx. 12% following moisture absorption for typical standard FR4.

Please note that thermal stress, such as that caused by soldering processes and thermal cycles, which the PCB undergoes during manufacture and use, can also affect the electrical and mechanical properties of the material. An increased temperature leads to thermal expansion, which can result in mechanical stresses and potential defects such as delamination or microcracks. These effects can compromise the reliability and longevity of the PCB. Therefore, when planning the multilayer structure, the thermal stresses to which the PCB will be exposed during use should also be taken into account.

A well-designed layer structure and the selection of suitable materials can help to minimise thermal stresses and extend the service life of the PCB:

- **High-temperature-resistant materials:** High-quality prepregs and laminates from leading manufacturers are better able to withstand thermal stresses.
- **Reinforced prepregs:** Prepregs with a high glass content offer better mechanical properties and greater thermal stability.
- **Symmetrical construction:** A symmetrical layer structure helps to distribute mechanical stresses evenly and minimise warping.
- **Optimised layer thicknesses:** Plan the thicknesses of the prepregs and laminates so that thermal expansion is minimised.
- **Sufficient spacing:** Ensure there is sufficient space between the copper layers to accommodate thermal expansion and prevent delamination.

10.3. Via protection classes and via-in-pad (IPC-4761)

Choosing the correct via plugging technique is crucial for soldering reliability and package density. We manufacture in accordance with IPC 4761:

- **Plugging (Type IIIa)**: Standard method for protecting vias. Up to a diameter of 0.45 mm, this is carried out via a process-optimised method of sealing with lacquer (**see details in Chapter 12**),
- **Via-in-Pad / VIPPO (Type VII – Filled & Capped)**: For high-end applications (e.g. BGA), we use complete filling followed by over-plating.
    - **Microfilling (Cu):** Copper filling for blind vias (≤ 0.15 mm, aspect ratio 1:1, **see Section 13.2.**),
    - **Resin filling**: Sealing for through-holes (0.1 – 2.0 mm, aspect ratio up to 10, **see Section 13.3**).

11. Circuit pattern creation

The lithographic limit for the resolution of circuit patterns (track/gap) in the exposure systems we use is the thickness of the dry resist to be exposed. If this has a thickness of 50 μm, the maximum possible resolution is also 50 μm. Physical processes in the subsequent electroplating and etching processes also act as limiting factors. Consequently, the greater the final copper thickness, the greater the degree of undercutting at the edges, which must be compensated for in the exposure parameters.

In principle, the reproducibility of a layout depends on its design and on the thickness of the copper structure. The technical restrictions of solder mask creation must also be taken into account. Here, during layout creation and editing, necessary considerations arise regarding the coverage, undercutting or even exposure of the conductor flanks and insulation areas.

Final copper thickness 35 μ	Standard μ		Special μ		Technical limit μ	
	Outer layers	Inner layers	Outer layers	Inner layers	Outer layers	Inner layers

Trace width	120	120	100	100	60	60
Track spacing	120	120	100	100	70	70
Restring	125	150	100	120	70	80
Registration accuracy	± 20 µ		+/- 15 µ		± 12 µ	
Final copper thickness 70 µ	**Standard µ**		**Special µ**		**Technical limit µ**	
	Outer layers	Inner layers	Outer layers	Inner layers	Outer layers	Inner layers
Trace width	150	150	125	125	100	100
Track spacing	170	170	140	140	120	120
Restring	180	200	150	170	120	120
Registration accuracy	± 20 µ		± 15 µ		± 12 µ	
End-cap thickness 105 µ	**Standard µ**		**Special µ**		**Technical limit µ**	
	Outer layers	Inner layers	Outer layers	Inner layers	Outer layers	Inner layers
Trace width	200	200	170	170	130	130
Track spacing	250	250	225	225	200	200
Restring	250	275	200	225	150	175
Registration accuracy	± 20 µ		± 15 µ		± 12 µ	
Final copper thickness 140 µ	**Standard µ**		**Special µ**		**Technical limit µ**	
	Outer layers	Inner layers	Outer layers	Inner layers	Outer layers	Inner layers
Trace width	300	300	250	250	230	230
Track spacing	400	400	360	360	320	320
Restring	300	300	270	270	250	250
Registration accuracy	± 20 µ		+/- 15 µ		± 12 µ	

12. Solder mask

12. Solder resist

In the photochemical solder resist process, the surface is embedded in a photosensitive polymer. The chemical cross-linking of the polymers is achieved through controlled exposure; all unexposed areas are developed with sharp contours, even at the micrometre level. To achieve the required electro-physical properties of the resist, a UV bump is subsequently applied – effectively a ‘glazing’ of the resist surface to reduce ionic contamination – followed by final thermal curing.

During solder mask coating, the solder pads of the via holes can be printed over on request. However, this does not guarantee the sealing of the via holes (via plugging) (unsuitable for vacuum testers).

If sealing of the via hole is absolutely essential, however, this is carried out using standard resins for hole diameters up to 0.45 mm**.** For flatness requirements (via-in-pad), we rely on filling with copper (**microfilling, Section 13.2**) or sealing by means of **resin filling (Section 13.3)**.

12.1. Parameters, clearance and expansion of solder resist

We use exclusively epoxy resin-based solder resist, as this additionally improves the creep resistance on the surface of the printed circuit boards.

Values apply to green solder resist	Standard μ	Special μ	Technical limit μ
Circular expansion of the solder resist mask	70	50	30
Minimum web width	80	60	50
Min. distance between SMDs*	200	170	150
Registration accuracy green/other	± 20/40 μ	± 15/35 μ	± 12/30 μ

*Minimum distance between solder mask-free areas required to reproduce a solder mask bridge

When creating solder mask patterns, solder mask cut-outs must be provided in a 1:1 ratio to the pads, i.e. without oversizing. We calculate the oversizing required for production ourselves.

The following solder mask colours are available:

- **green (standard)**
- blue
- black
- red
- white

TOP/BOTTOM can be painted in different colours.

13. Electrolytic copper deposition process

13. Electrolytic copper plating process

The thickness of the copper plating depends on the exposure time and the current in the electroplating bath.

Generally, a copper deposit of 20 µm to 25 µm is applied to the surface and within the through-holes during the process. Thicker copper layers can be achieved by adjusting the process parameters or using additional electroplating processes.

To achieve uniform copper deposition, the layout design should ensure that conductor track structures are either not embedded in ground at all, or are fully embedded in ground. The conductor tracks and pad positions should be centred within a ground embedment and spaced at equal intervals from one another. If copper structures are unevenly distributed in the layout, there is a tendency for over-deposition to occur in the 'ground-poor' regions. This leads to a reduction in trace spacing, potentially resulting in electrical failure due to short circuits, as the traces effectively grow together. For micro-vias (unfilled): metallisation in the via ≥ 12 µm (guide value).

Copper foil μ	Electrolytic copper deposition	Final copper thickness
18 μ	approx. 20 μ	approx. 35 μ
35 μ		approx. 55 μ
50 μ		approx. 70 μ
70 μ		approx. 90 μ
85 μ		approx. 105 μ
105 μ		approx. 125 μ

13.1. Aspect Ratio

For through-holes and buried vias, the ratio of 'material thickness to hole diameter' is defined. It is calculated as follows: material thickness divided by the smallest hole diameter.

Example: 1.6 mm material thickness divided by 0.2 mm hole diameter = 8

Standard	Special	Technical limit
8	10	> 10

This value is crucial for the manufacturability of the printed circuit board, as the higher the aspect ratio, the more complex it is to produce metallisation in the holes.

For blind vias and micro-vias, the aspect ratio is calculated as drill depth (layer spacing) ÷ hole diameter; limit value ≤ 1 : 1.

13.2. Microfilling (Via-in-Pad)

This technology enables the simultaneous filling of blind vias and the reinforcement of through-holes.

In HDI circuits, there is usually not enough space to route signals to different layers via through-holes. A space-saving solution is Via-in-Pad: blind vias are positioned directly in SMD pads and filled with copper after drilling; the planarised surface aids the soldering process. Example (fine-pitch): BGA/CSP/flip-chip zones with Via-in-Pad for short transitions and uniform paste distribution. Due to this filling, only a very small amount of solder flows into the remaining 'dimple' and enables a proper solder joint. Target value for the dimple: ≤ 25 µm. (Guideline according to ZVEI). The maximum drill diameter is 0.15 mm.

13.3. Via Plugging (Resin Filling / VIPPO)

Sealing both through-holes and blind vias with resin, followed by over-plating, is an alternative to microfilling; however, this process is more complex in terms of process technology. Resin filling followed by over-plating corresponds to filled and over-plated Via-in-Pad solutions (VIPPO / IPC-4761 Type VII).

The advantages over microfilling are that through-holes ranging from 0.1 mm to 2 mm can also be filled. The material thickness must not be less than the hole diameter.

14. Surface Finishing

We are currently able to provide the following surface finishes:

- Lead-free hot-air tinning (HAL) – Sn / 0.3 Ag / 0.7 Cu / 0.02 Ni
- Electroless nickel-gold (ENIG) – 99.9 Au
- Electroless nickel-palladium-gold (ENEPIG)
- Chemical tin (chem. Sn)
- Chemical silver (chem. Ag)
- Organic tarnish protection (OSP)
- Electrolytic nickel-gold (hard and bond gold) – hard 99.8 Au / soft 99.99 Au

Properties of the various finish surfaces:

	HAL	ENIG	ENEPIG	Chemical Sn	chem. Ag	OSP	electroplated Au
Coating thickness µ	< 10	0.05–0.12 Au 4–8 Ni	0.03–0.10 Au 3–7 Ni	0.80–1.20	0.15–0.45	0.02–0.06	0.80–5.00

			0.08–0.30 Pd				
Flatness	+	++	++	++	++	++	++
Shelf life under stable conditions	< 12 months	< 12 months	< 12 months	< 6 months	< 6 months	< 6 months	< 12 months
Repeat solderability	++	++	++	limited*	+	o	yes (soft)
Can be reactivated	yes	conditionally*	conditional*	yes	No	yes	no
Al wire bonding	no	yes	yes	no	conditional*	no	yes (soft)
Au wire bonding	no	no	no	no	no	no	yes (soft)
Push-button contact	no	yes	yes	no	no	no	yes
Press-fit technology	yes	no	no	yes	yes	no	no

*only possible to a limited extent under specified conditions.

15. Printing techniques

15.1. Serialisation

To ensure that printed circuit boards can be uniquely identified, individualised marking of the individual boards within a series is also an option. This marking is applied automatically (direct exposure of the structures or assembly printing) in white and may consist of static information (e.g. production date, date code, etc.) and sequential numbering in chronological order, and can be displayed in the following machine-readable formats:

- **1D & 2D barcodes, Data Matrix, QR codes.**

15.2. Marking print / assembly print

To avoid interruptions or obscuring within the print image, the line width of the marking print should not be less than 130 µm and the font height should not be less than 1000 µm. The solder pads should be left free of the marking print by at least 250 µm all round, as otherwise an unclean print image and printing onto the solder pads is possible.

	Standard µ	Special µ	Technical limit µ
Distance between print image and pad	200	150	100
Distance between print image and holes	200	150	100
Line thickness	130	100	75
Font size	1000	750	500
Registration accuracy	± 200 µ	+/- 150 µ	± 70 µ

15.3. Carbon printing

	Standard µ	Special µ	Technical limit µ
Distance between carbon surfaces	500	400	300
Minimum width of the carbon surface	700	600	500
Registration accuracy	± 250 µ	± 200 µ	± 150 µ

15.4. Stripping varnish

The layer thickness of the peelable lacquer is approx. 500 µ.

Holes covered with peelable lacquer should not exceed 1.8 mm in size.

	Standard	Special	Technical limit
Maximum bridgeable diameter	1.8 mm	2.0 mm	2.6 mm*
Minimum width	6 mm	5 mm	4 mm
Registration accuracy	± 300 µ	± 250 µ	± 200 µ

*Full bridging of the hole cannot be guaranteed.

16. Contour machining

16. Contour machining

We drill, mill and score your printed circuit boards according to your specifications and requirements. The type of mechanical machining depends on your individual specifications. In our drilling and milling centre, we work with modern, fully automatic CNC drilling and milling machines. These techniques enable machining in accordance with the DIN 7168 standard: “medium” (medium accuracy) and “fine” (precise accuracy).

If non-plated-through holes are positioned within a solder pad, the pad must be at least 500 µm larger in circumference than the hole. Otherwise, solder pads may be removed.

If no information regarding the type of holes is provided for through-hole printed circuit boards, we will determine independently, to the best of our knowledge, which holes are through-holes and which are not.

If drilling or dimensional drawings are provided that do not correspond to the drilling programmes or the outline as per the layout data, the drilling programmes and the outline as per the layout data shall in all cases be binding for production.

Unless otherwise specified, the centre point (= centre vector) of the contour lines in the layout data is decisive for the contour of the PCB. If slots are represented by rectangular contours, we assume that the corner radius is included.

Depending on the size of the printed circuit boards, the following tolerances are specified (other tolerance values are possible by agreement):

Format mm	Medium mm	Fine mm
0.5–6	+/- 0.10	± 0.05
6–30	± 0.20	± 0.10
30–120	± 0.30	± 0.15
120–400	± 0.50	± 0.20
400–1,000	± 0.80	± 0.30

16.1. Scoring (notching)

The angle of the scoring blades is 15°. Therefore, along the contours being scored, a distance between the conductor tracks and the contour must be maintained in accordance with the following table:

Material thickness mm	Distance between conductor tracks and the contour mm
up to 1.00	0.45
1.10 – 1.60	0.50

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Material thickness mm	Distance between conductor tracks and the contour mm
1.70–2.00	0.70
2.10–2.50	0.80
2.60–3.20	1.00

If no positive tolerance is permitted for the contour, the desired negative tolerance must be added to the above-mentioned values for ‘Distance between traces and contour’.

Example: PCB format 100 mm x 100 mm +0.00/-0.30 mm

Distance between traces and contour for 1.6 mm material thickness: 0.5 mm + 0.15 mm = 0.65 mm

16.2. Milling

As an alternative to scoring, we offer contour milling. The advantage over scoring is that the outer contours can be machined into the most intricate shapes and cut-outs, such as round, oval, wave-shaped, zigzag, etc.

Please note the following regarding milling:

- If delivery is to be in a milled panel, a standard spacing of 2.0 mm between the PCBs is sufficient to allow milled bridges to be placed between the individual boards.
- If delivery is not to be in a panel, a spacing of at least 8.0 mm between boards must be allowed for, so that the PCBs can ultimately be separated.

16.3. Deep milling and drilling / countersink holes

Milling and drilling with a defined Z-axis are carried out in accordance with your drawing specifications. Countersinks are produced as standard at 45° or 30°. The specifications for this can be customised.

16.4. Milling and scoring combination

In some cases, it makes sense to combine both milling and grooving to achieve the best balance between cost and material loss. Our CNC machines are capable of executing these combinations with precision.

16.5. Chamfering

To facilitate the assembly of plug-in contacts (e.g. PCI connectors), edge chamfering at 45° or 30° is possible at varying depths.

16.6. Edge metallisation

To create edge contacts, we can produce special edge metallisation (e.g. side plating or castellated holes). This is particularly useful when improved electrical conductivity or shielding is required.

16.7. Semiflex

In the semi-flex technique, a defined area of rigid PCBs is milled down to a residual material thickness to allow the material to be bent there. Although the same bending angles and radii cannot be achieved as with rigid-flex circuits, they are often sufficient for the applications. Depending on the design, the Semiflex technique allows for three to five bends; the PCB must therefore be statically mounted.

The main advantages lie in the lower manufacturing costs and the elimination of the otherwise necessary polyimide film, which in turn would require thermal pre-treatment due to its high moisture absorption.

17. Drilling and milling tolerances

Through-hole (PTH)		Standard mm	Special mm	Technical limit mm
Smallest drill diameter		0.35	0.15	0.10
Maximum drilling diameter		6.00	6.00	6.00
Minimum distance between drill tangents*		0.20	0.15	0.075
Minimum distance between the hole tangent and the conductor track*	Outer layers	0.20	0.15	0.075
	Inner layers	0.25	0.20	0.10
Surface Hot air levelling Tin plating Tolerance	Final diameter <= 6 mm	+0.10/-0.05	+0.09/-0.06	+0.08/-0.05
	End diameter > 6 mm, milled	+0.14/-0.05	+0.10/-0.05	+0.08/-0.05
Surface OSP/ENIG/chemical tin/silver Tolerance	End diameter <= 6 mm	+0.10	+0.05/-0.05	+0.10
	End diameter > 6 mm, milled	+0.12/-0.02	+0.06/-0.06	+0.10

Hole position tolerance of plated-through holes relative to non-plated-through holes and to the contour	+/-0.20	+/-0.07 **	±0.05 ***

Non-plated-through holes (NPTH)		Standard mm	Special mm	Technical limit mm
Smallest drill diameter		0.40	0.20	0.15
Maximum drilling diameter		6.40	6.40	6.40
Minimum distance between drill tangents*		0.20	0.15	0.10
Minimum distance between the drill tangent and the conductor track*	Outer layers	0.20	0.15	0.05
	Inner layers	0.25	0.20	0.10
Tolerance	Final diameter <= 2 mm	+/-0.05	+/-0.03	±0.03
	End diameter 2 <= 6 mm	+0.1/-0.05	±0.05	±0.03
	End diameter > 6 mm, milled	+0.1/-0.05	+/-0.06	+/-0.04

*Please note that through-holes must generally be drilled or milled 150 µm larger than the desired final diameter to compensate for the metallisation in the hole. For example, if you require a final diameter of 0.6 mm, the diameter of the drill bit used is 0.75 mm, unless different tolerances are specified.

**depending on the hole diameter

***provided that the drilling process is carried out in a machine clamping (tenting)

18. Storage

18.1. Humidity

Due to the epoxy resin in the base material of the printed circuit boards, these (particularly multilayers) are extremely hydrophilic; i.e. water molecules dissolved in the air are absorbed by the material. Depending on the ambient conditions, moisture equilibrium is established in the materials. Under storage conditions of, for example, 20 degrees Celsius and 35 per cent humidity, moisture absorption of 0.12 per

cent (by weight of the epoxy resin) is already recorded after 12 days. The crucial factor here is that as moisture absorption increases, so does the gas pressure within the printed circuit board, which is caused by the high temperatures during the soldering process. If moisture absorption exceeds 0.17 per cent, a critical gas pressure of 8–10 bar is reached, at which point delamination and blistering may occur. Epoxy resin can absorb up to 0.5 per cent by weight of moisture.

To ensure that the moisture content and the adhesive bond of the material are flawless, we carry out a delamination test on a test specimen after the completion of multilayer printed circuit boards.

To further prevent or reduce moisture absorption, we strongly recommend the following:

Storage environment

PCBs should be stored in a constantly heated environment under controlled conditions until shortly before soldering/processing, preferably in darkened rooms. Due to climatic changes, a controlled storage environment is becoming increasingly important to preserve the quality of the printed circuit boards. Humidity and temperature fluctuations should be minimised, and the packaging of the printed circuit boards must be checked for integrity before processing.

We strongly recommend that you adhere to the following storage conditions to minimise moisture absorption:

- Room temperature 18–21 °C
- Relative humidity < 50%

Packaging

Storage should preferably take place in sealed containers. Please note that polyethylene bags do not provide reliable protection against moisture due to their water vapour permeability. To improve protection, we therefore also offer the option of packaging the printed circuit boards in DRY-SHIELD protective bags. It is also possible to vacuum-seal them and/or fit them with indicators and desiccant sachets. The protective films/bags should only be removed shortly before soldering/processing. We recommend re-vacuum-sealing any remaining quantities, or at the very least sealing them securely with adhesive tape or by tucking the film between the printed circuit boards, and storing them in boxes to prevent draughts.

Storage period

The storage period for printed circuit boards should be as short as possible, and consumption should follow the ‘first-in, first-out’ principle. For storage periods exceeding 3 months (from the date of production), it is difficult to predict when moisture absorption may begin to cause problems during soldering/processing due to a wide variety of influencing factors such as layout, layer structure, etc. To provide reliable proof of storage duration, we can apply a production date/date code to the printed circuit boards by arrangement. Please note that shelf life also depends on the chosen surface finish. You will find indicative values for this in the Surface Finishing section of this document. Please always use opened packages first.

18.2. Soldering test

PCBs that have already been in storage for several months and whose transport conditions are unclear (goods transported by freight forwarders in all weathers and temperatures) should definitely be subjected to a soldering test before further processing.

18.3. Pre-conditioning/drying

To reduce the moisture absorbed, we recommend drying the goods in an oven regardless of the outcome of a solder test, whereby the PCBs should preferably be dried vertically in a rack. If you store the PCBs with us for more than four months (e.g. for orders on call), we will dry them before dispatch in any case.

Degree °C	Drying time
120	4 hours
110	6 hours
100	8 hours

If drying in a vacuum oven at 50 mbar is possible, the temperature can be reduced by approx. 20 °C and the time by approx. 30 minutes. This method is advantageous for the sensitive ‘chemical tin’ surface. Subsequently, a few test samples should be used to determine whether the solder still wets sufficiently; otherwise, the chemical tin must be refreshed.

After drying, processing of the printed circuit boards should commence immediately, as the hydrophilic properties of the board remain. The time between the various soldering processes must be kept as short as possible and should not exceed 8 hours. This is the only way to prevent excessive moisture absorption in unprotected material. Dried and tempered printed circuit boards will experience short-term saturation with water from the ambient air.

18.4. Product-specific requirements

The values mentioned in the preceding sections are guide values.

These values do not fully account for the different processing parameters and product-specific properties of individual printed circuit boards and must be determined on a product-specific basis by the respective processor:

- Different soldering processes and profiles result in varying levels of stress. For example, the thermal stress in convection ovens is not as high as in infrared ovens or vapour-phase systems.
- If the recommended storage conditions cannot be maintained consistently, the material will absorb more water than is possible under constant conditions. Packaging in DRY-SHIELD protective pouches can help to remedy this.
- If the layout contains large, closed copper areas, it takes longer for the moisture to escape.
- The multilayer structure. See: 10.2. Consideration of physical influencing factors